PHASE 2 OF THE ARRAY AUTOMATED ASSEMBLY TASK FOR THE LOW COST SILICON SOLAR ARRAY PROJECT

INTERIM REPORT

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"The JPL low-cost Silicon Solar Array Project is sponsored by the U.S. Department of Energy and forms part of the solar Photovoltaic Conversion Program to initiate a major effort toward the development of low-cost solar arrays. This work was performed for the Jet Propulsion Laboratory, California Institute of Technology by agreement between NASA and DOE."

Approved: Jack R. Anderson

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

1. Introduction

The LSA Automated Array Assembly Task has as its goal the manufacture of photovoltaic modules at a capacity of 500 MW per year at a cost of $0.50 per peak watt. Divided between ten solar cell manufacturers, each installation should produce 50 MW per year. This implies that automated machinery would continuously produce 120 solar cells per minute. The purpose of this report is to detail the processes and techniques which we believe to have great promise of accomplishing this task.

The initial stages of the program were involved in studying the possibility of automated assembly. Phase 1 reviewed a large cross section of processes, conceptual designs, and innovative technologies in preparation for 1986. Through this documentation, a large amount of comprehensive data has been collected. It is these reports upon which the next phase of the program is based.

The purpose of Phase 2 is to propose an automated sequence, verify it and present future cost projections. Utilizing the large amount of information available from Phase 1 and drawing from its own experience Solarex has proposed a process sequence which we believe has great potential of achieving the LSA goals. This report will describe the processes, detail the verification tests performed, and estimate the cost of such an automated array assembly.

In order to stay within the boundaries of the program, a variety of innovative technologies were developed. Techniques such as non-vacuum application of aluminum backs, negative screen printing, and the interconnection scheme are examples of such innovations. By spraying the positive contact of the wafer, the use of large and sophisticated machinery has been eliminated. Screen printing is a well known technique for applying front metal contacts to solar cells. The application of a negative image on the cell, however, represents a large cost savings over the more conventional method. Likewise, the interconnection scheme of arc-spraying tabs directly on glass and reflowing the cells onto it, is an efficient way of replacing the human operation of tabbing. In general, the entire operation has been designed to operate at room atmosphere on a continuous flow basis avoiding batch processing wherever possible.

The results of the program demonstrate that the feasibility of an automated production facility is very high. The processes, as described in this report, have yielded 9.5% efficient solar cells. In an automated environment it is expected that the process can be optimized to produce even higher efficiencies at a rate of about 2 panels per minute. In addition, the overall cost estimates of the process (49.75¢/wafer) represents a tremendous savings over current module

production prices. Therefore, it is our conclusion that automatic fabrication of efficient low cost photovoltaic modules can be effected in 1982, rather than 1986 as previously predicted. The responsibility of making these low costs modules available rests both on the government and private industry.

2. Surface Preparation

The surface of the fresh cut wafers contains damage from the sawing operation, which has a detrimental effect upon the future electronic performance of the cell. In order to remove this work damage and prepare the wafer for efficient solar cell operation, the wafers are chemically etched in sodium hydroxide solution. In order to capture a large percentage of the incident insolation the wafers are textured to form a pyramid surface. This is accomplished by a chemical etch with a potassium hydroxide solution. Both of these etching processes are well known at Solarex and require little or no verification work. In addition, chemical etching is cost effective and readily automatable with existing product handling machinery such as moving belts and baskets.

The proposed scheme of surface preparation begins with a NaOH etch to correct the sawing damage. The etch rate of silicon is shown for varying temperatures in Figure 2.1 at 25% concentration of NaOH. It can be seen that as the temperature of the bath is increased the etch rate (μm/min) increases almost exponentially. Most of the surface can be etched quickly in a hot etch. Agitation in the bath is assured by the etch reaction itself which results in substantial effervesence. The critical parameters of the etching process in hot NaOH are the temperature of the bath, the concentration of the solution, and the orientation of the silicon crystal.

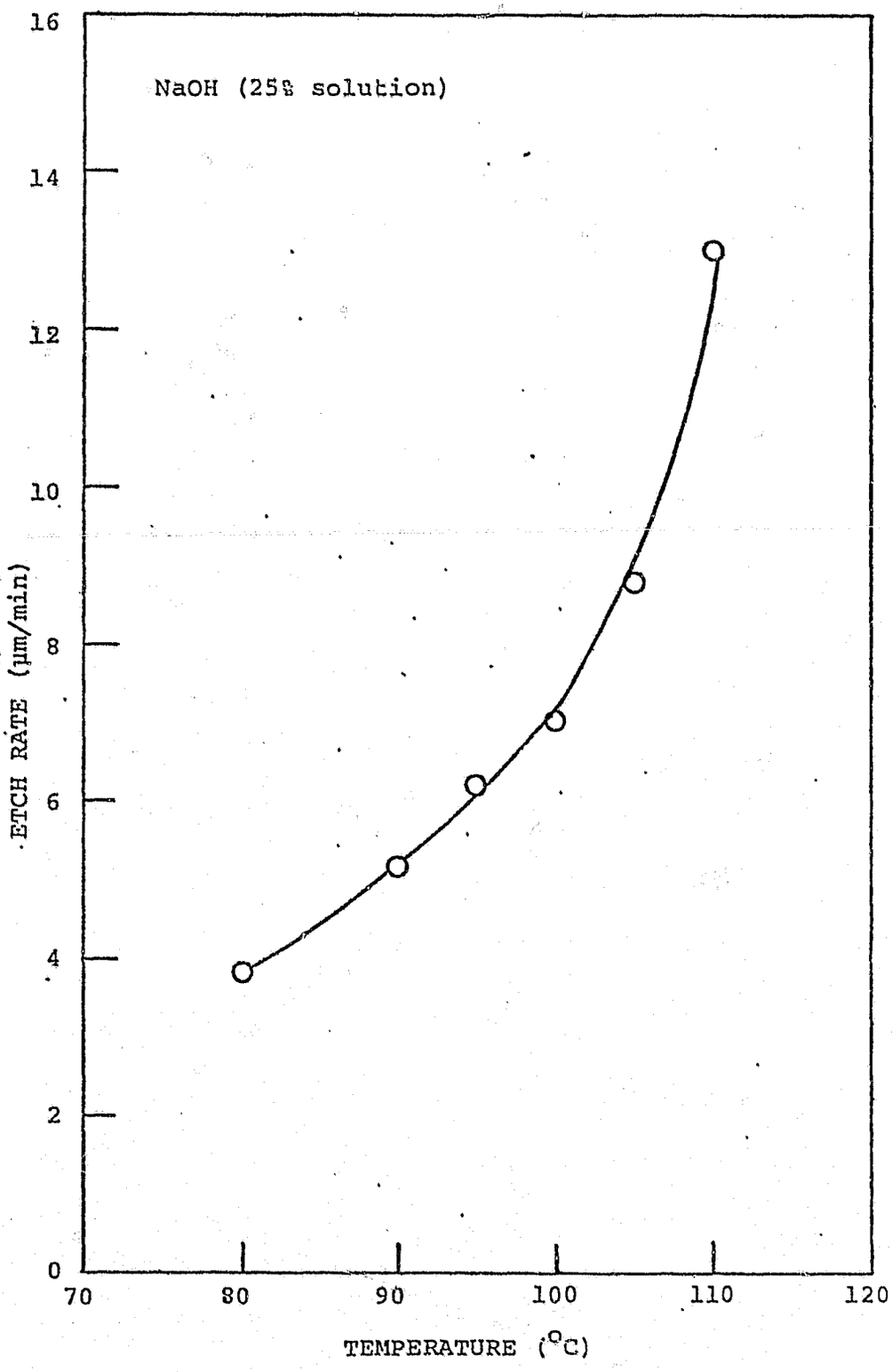


Figure 2.1 Etch Rate of NaOH at Varying Temperatures

The 1-0-0 orientation is the one which is most commonly used for normal production because the degree of texturing can be varied. The surface of the wafer can be varied from a smooth surface to a highly textured surface. A textured surface has increased light absorptivity which augments the overall efficiency.

Solarex has elected to subject the wafers to a second etch bath consisting of KOH to produce a pyramid surface. The effect of a textured surface on the optical reflection is shown in Figure 2.2. The graph compares four uncoated surface conditions which range from a smooth polished surface to a pyramid surface created by KOH. A 100% reflection curve is drawn as a reference as well as an evaporated Ta_2O_5 anti-reflective (AR) coating curve for comparison. The graph shows that the pyramided, KOH 2% sample has a very low reflection coefficient. The etch variables that produced these wafers, and three others, are presented in Table 2.1. This table clearly demonstrates the high absorption properties of the KOH etching process.

The economic evaluation of the etch process for both sides of the wafer is based on a throughput rate of 120 wafers per minute and a process duration of 15 minutes. It is estimated that the overall cost of surface preparation will be 1.48¢ per wafer, including materials, equipment, overhead and labor.

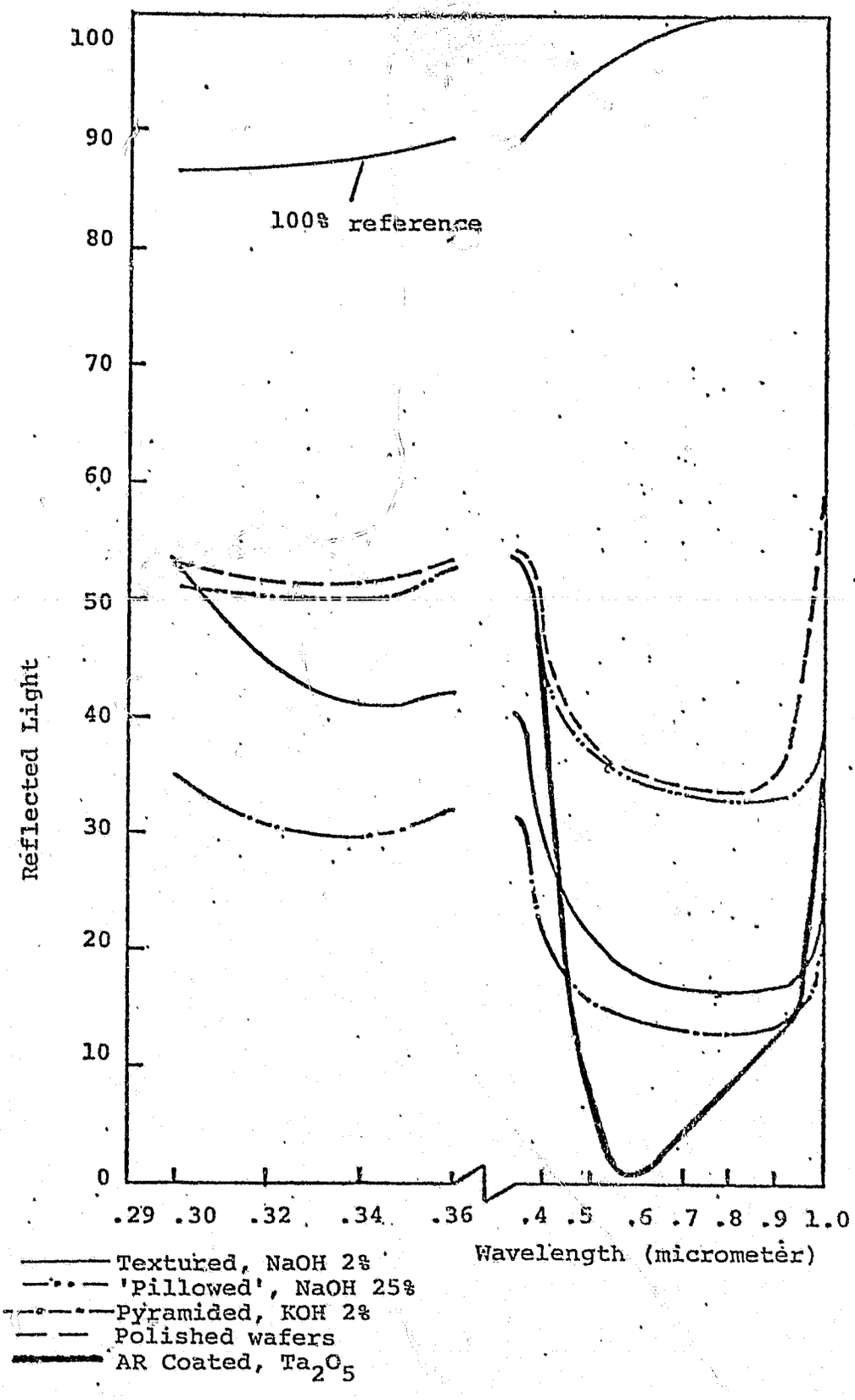


Fig.2.2 Reflection from Silicon Surfaces
Copy of chart recording.

Surface Crystal Orientation	Surface Texture Before Etch	Etch Solution	Temperature And Time	Alpha* And Surface Texture
1-0-0	Mirror Polish	✓ NaOH 2%, 2-Propanol 35%	85°C, 50 min.	0.76 Textured
1-0-0	Fine Grit Smooth Finish	NaOH 2%, 2-Propanol 35%	85°C, 50 min.	0.72 Textured
1-0-0	As Cut	NaOH 2%, 2-Propanol 35%	85°C, 50 min.	0.73 Textured
1-0-0	Fine Grit Smooth Finish	KOH 2%	75°C, 15 min.	0.77 Pyramided
1-0-0	Fine Grit Smooth Finish	✓ NaOH 25%	105°C, 10 min.	0.56 Pillowed
1-0-0	As Cut	✓ KOH 2%	85°C, 20 min.	0.81 Pyramided

*Alpha is the average surface absorption weighted over the AM2 spectrum.

✓ Shown in Fig. 2.2

Table 2.1 SILICON PREPARATION - SURFACE TEXTURE

Based on the large amount of experience obtained at Solarex, surface preparation can be considered a fully developed and readily automatable process sequence. Surface texturing is a good method of reducing the cell reflectivity, and has the advantage that elaborate and expensive vacuum processes for AR coating can be avoided.

3. Junction Formation

The process of junction formation converts the silicon wafer into a solar cell. Dopant material is applied and diffused into the silicon creating the P-N junction of the cell. The negative side or face of the wafer is doped with SX-101 and diffused. The back is formed by alloying metal to the opposite side of the cell. Junction formation requires careful control of time, temperature and dopant concentrations to produce high efficiency solar cells. An extensive amount of experimental work has been carried out, in order to determine these parameters for a low cost, high throughput automated production line. We are now confident that this junction formation technique is well suited to an automated environment, which yields cells with good electrical characteristics.

The process consists, firstly, of applying the dopant SX-101 (phosphoric acid and ethyl alcohol) on the wafer and spinning it at 10,000 rpm to regulate the dopant quantity. Then the wafers are passed through a low temperature furnace (150°C) for drying and preheating. This is followed by exposure to a high temperature furnace (950°C) for 6 minutes to complete the diffusion process. During this process, oxides form on the surface which are removed with a buffered HF solution. A back contact is formed by alloying aluminum into the bulk silicon. The back side of the wafer is sprayed with aluminum powder suspended in an organic fluid. The process is completed by alloying the wafers at 650°C for 6 minutes.

The determination of the five parameter system including dopant type, dopant quantity, spin speed, diffusion temperature, and wafer surface texture, was accomplished by a large amount of experimentation. The choices were narrowed to three dopants, Emulsitone's N-250, Allied Chemical's PX-10, and Solarex's SX-101. The SX-101 dopant was chosen not only because of the favorable results obtained, but mainly due to the significant cost savings achieved in comparison to the other commercial products. Solarex's SX-101 costs about 2¢ per wafer which yields a cost of less than 5¢ per wafer for the overall junction formation process. During the experiments mentioned above, the diffusion time was held constant at 9 minutes, which is longer than our present diffusion time. Therefore, any interpretations made from these results should take this into account.

Dopant quantity has also been a topic of experimentation for two spin speeds 3000 and 10,000 rpm. Table 3.1 indicates the maximum amount of dopant material required to completely cover the wafer. The results indicate that textured wafers seem to require slightly more dopant material than the pillowed one, (0.7 cc as compared to 0.4 or 0.6 cc), for both spin speeds. The wafers were diffused and classified according to their resulting sheet resistance. Those wafers which resulted in sheet resistance between 50 $\Omega/\square$ and 150 $\Omega/\square$ were made into solar cells using the conventional cell making process. The electrical characteristics of these cells can also be seen in

Dopant: Solarex SX-101

Diffusion: 950°C, 9 minutes

Surface: Pillowed, 1-0-0

Amount	RPM	V_{oc} mV	I_{sc} mA (2 x 2cm)	$Power_{max}$ mW (AM1)
.4cc	10K	580	98 ± 1	42 ± 1
.6cc	3K	585	99	44 ± .5

Dopant: Solarex SX-101

Diffusion: 950°C, 9 minutes

Surface: Textured, 1-0-0

Amount	RPM	V_{oc}	I_{sc} (2 x 2cm)	$Power_{max}$ mW (AM1)
.7cc	10K	580	125 ± 2	54 ± 1
.7cc	3K	590 ± 2	127 ± 2	56 ± 2

TABLE 3.1

Table 3.1. Peak power from these cells compare very favorably with other cells which utilize a more commonly used doping method. It can be deduced, therefore, that dopant quantity is not critical as long as the entire wafer is coated.

Another measurement performed was the quantum yield of 4" diameter cells. The quantum yield measurement is the ratio of charge carriers generated in the external circuit to the number of photons absorbed. It is measured by illuminating the cell with spectrally narrow light. By knowing the wavelength and the intensity, the number of incident photons per second can be derived. This value is compared to the number of generated charge carriers per second, which is directly proportional to the short circuit current. The ratio of incoming photons to short circuit current generated must be corrected for reflection losses. The curve, presented in Figure 3.1, takes this correction into account.

The spectral response of textured cells with junctions formed by spin-on dopants compares well with textured cells whose junctions are are formed by gaseous diffusion.

In summary, our technique for junction formation has provided good results which are comparable to the more commonly used diffusion processes. In addition, this technique presents no compatibility problems between process steps, and has a high rate of reproducibility. In other words, it lends itself well to an automated sequence.

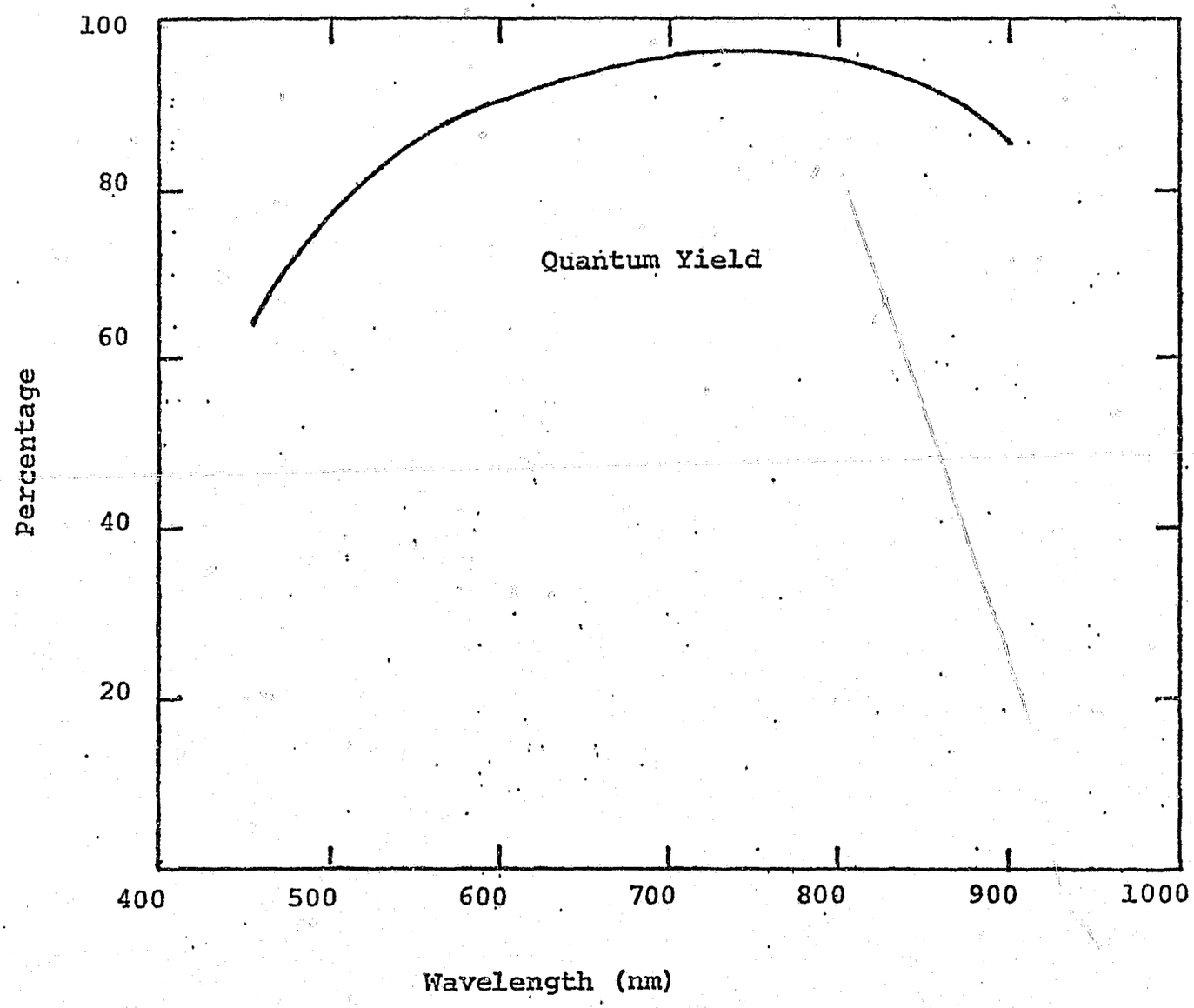


Figure 3.1 Quantum Yield for textured cell, Spin-on Dopant

4. Cleaning - Post Diffusion Etch

In preparation for the metallization step the surface of the wafers must be etched to remove oxides and residual dopant material. As the wafers leave the junction formation stages they have uneven surfaces, surplus aluminum powder, and other contaminates which must be removed. This is accomplished by exposing the wafers to a dilute bath of hydrofluoric acid in which the critical parameter is bath duration.

The process sequence consists of loading the wafers into a fluoroplastic holder and immersing them in 10:1 HF solution at room temperature for 1 minute. Due to the effervescent reaction between aluminum and HF no mechanical scrubbing is required.

Some of the preliminary work done with this process was directed towards finding the right combination of parameters to clean the wafers until they became hydrophobic. As a result, a large number of experiments were performed in which diffusion temperatures, HF bath concentrations, and bath duration were varied. The findings are summarized in Table 4.1 for the SX-101 dopant only. It has since been determined that there is no need for the wafers to be hydrophobic. Efficient cells can be made with only a moderate cleaning.

This process step can be readily carried out in an efficient automated manner. As in surface preparation, machinery is available which passes loaded wafers through liquid etch

DIFFUSION SOURCE REMOVAL

Pillowed Surface

Diffusion Source	Diffusion Temperature °C	Time in 20:1 HF	Time in 10:1 HF	Scrubbing Required?
SX-101	850	20 min.	0	Yes
SX-101	900	30 min.	0	Yes
SX-101	950	30 min.	5 min	Yes
SX-101	1000	30 min.	0	Yes
SX-101	1050	40 min.	0	Yes

Textured Surface

Diffusion Source	Diffusion Temperature °C	Time in 20:1 HF	Time in 10:1 HF	Scrubbing Required?
SX-101	850	0	30 min.	Yes
SX-101	900	0	30 min.	Yes
SX-101	950	0	30 min.	Yes
SX-101	1000	0	30 min.	Yes
SX-101	1050	0	30 min.	Yes

TABLE 4.1

stations, rinses, dries and places the wafers on belts. One crucial parameter of the belt transport system is to assure that all wafers leaving the etch station are facing upward in preparation for the metallization step. The belt will include, at the end of the process, a simple base system to optically identify the front or back of the cell and correct its position if necessary. This process is also very cost effective, where the total cost for this step is estimated to be about 0.26¢ per wafer; the major cost being the acid.

5. Metallization

After formation of the junction of a solar cell, both the active surface and the back surface of the cell requires a conductive material to collect and transport the cell current to the external load. This is customarily accomplished by metallizing the surface of the cell with thin metallic fingers so that they do not cover or shade too much of the cell. Usually a separate operation is required for the back metallization. Various schemes exist within the industry to accomplish this.

To follow the project philosophy, an innovative technology is required to produce front contacts in a cost effective and automated fashion. All forms of metallization through the use of vacuum deposition do not seem suitable for large scale production. This technique, though excellent for producing fine line patterns, is a batch type and time consuming process that requires large capital investment. Solarex's metallization technique is inherently low in cost and can be easily adapted to an automated sequence. It consists basically of three process steps: 1) negative silk screening, 2) electroless nickel plating, and 3) solder dipping. An added benefit of this process is that the back is metallized simultaneously with no added effort.

A description of the entire process will be reviewed in this section followed by a description of the verification work that has been done to prove the suitability of the process.

Metallization begins by employing the screen printing technique with a slight modification. Screen printing is a very attractive method of masking prior to metallizing solar cells in a high production environment. There is no need for vacuum systems or large capital investment. The proposed process involves printing a "negative" of the metallization pattern directly onto the surface of the wafer. In this way, the use of expensive metal based inks can be avoided. Polyurethane, a very inexpensive resist, is used to cover all those areas of the wafer which are not to be metallized. The grid lines of bare silicon are then left exposed to be nickel plated. It is expected that this process can be easily adapted to an automated line. A screen print machine can accommodate nine 4" cells each cycle. A cycle can be accomplished in four seconds which includes one second for printing and three seconds for loading and unloading.

The wafers are then exposed to an electroless plating solution which establishes the metal to silicon interface. A nickel solution, composed of nickel chloride and sodium hypophosphite is kept agitated and at a temperature of 90°C. The cells are dipped in this solution for 6 minutes. The nickel will adhere to the exposed bare silicon and form an ohmic contact. The cells emerge from this bath with thin coating of nickel in the desired finger

pattern. Once dry, the polymer applied during silk screening is dissolved in an organic washing agent leaving only the nickel line pattern.

This electroless nickel system has a few advantages over other plating techniques, the most noteworthy of these being that it does not use electrodes. Contact plating replaces the outside source of current with an internal galvanic couple, which provides the required flow of electrons. In electroless plating a chemical reducing agent is used to deposit the metal rather than an electric current. In addition, electroless nickel deposits are harder and more abrasion-resistant than electrolytically deposited nickel. Deposit uniformity is also very good especially into recesses, such as a textured surface. A graph of the effect of temperature on plating rate is presented in Figure 5.1 At our plating temperature of 90°C (+ 5°C, - 0°C) the rate of plating is increasing exponentially.

Once plated, the wafers are sintered, as will be discussed later, then the circumferences of the wafers are ground to eliminate any short circuit between the positive and negative terminals. During metallization, the metal on the back contact will overlap onto the front portion of the cell and causes an electrical short between front and back. This is illustrated in Figure 5.2 where the circled

EFFECT OF TEMPERATURE ON PLATING RATE,

ELECTROLESS NICKEL

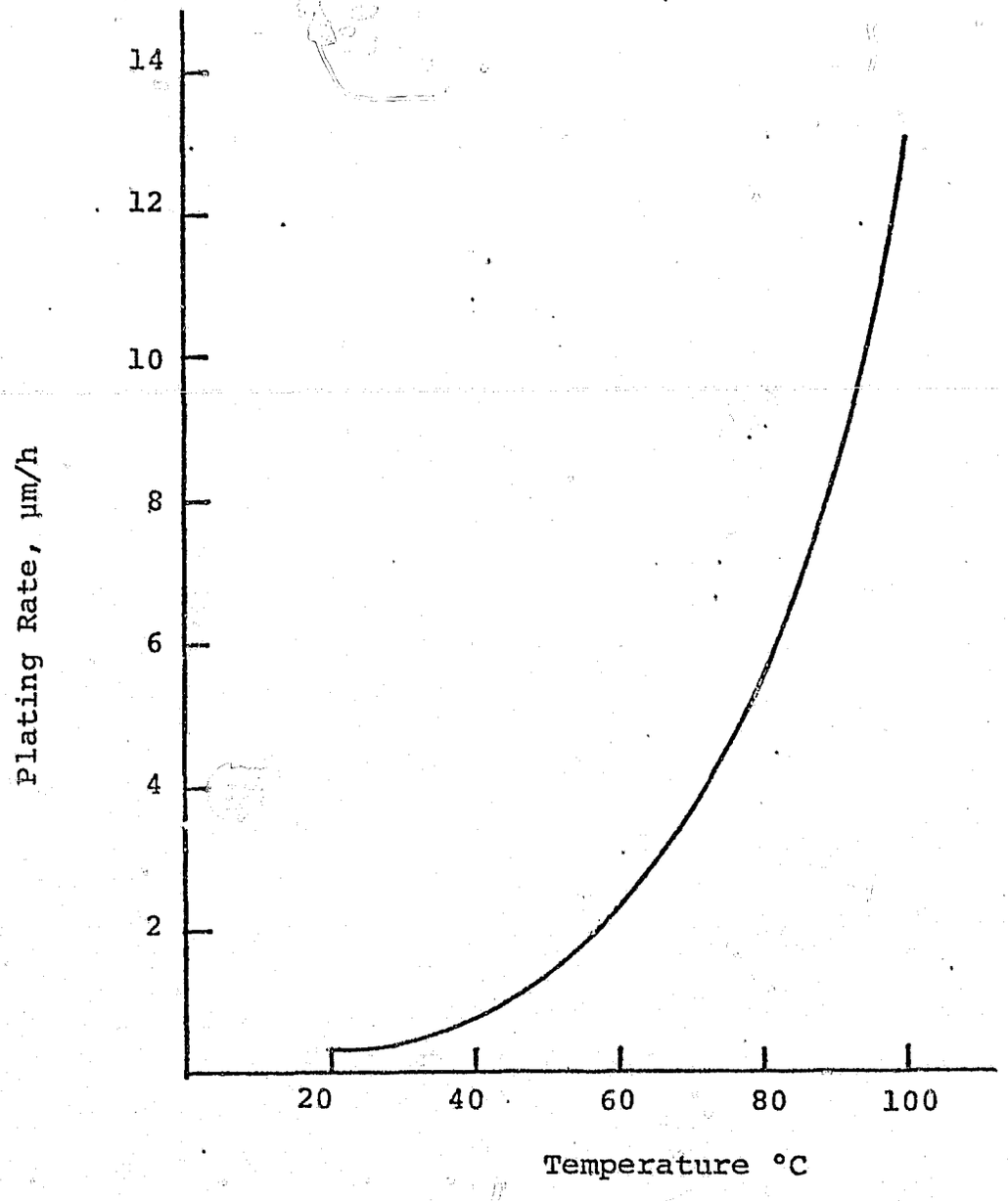


FIGURE 5.1

region depicts the shorted section. The elimination of the short is accomplished by grinding down the metal and silicon to the dotted line in the figure which corresponds to about two thousanths of an inch.

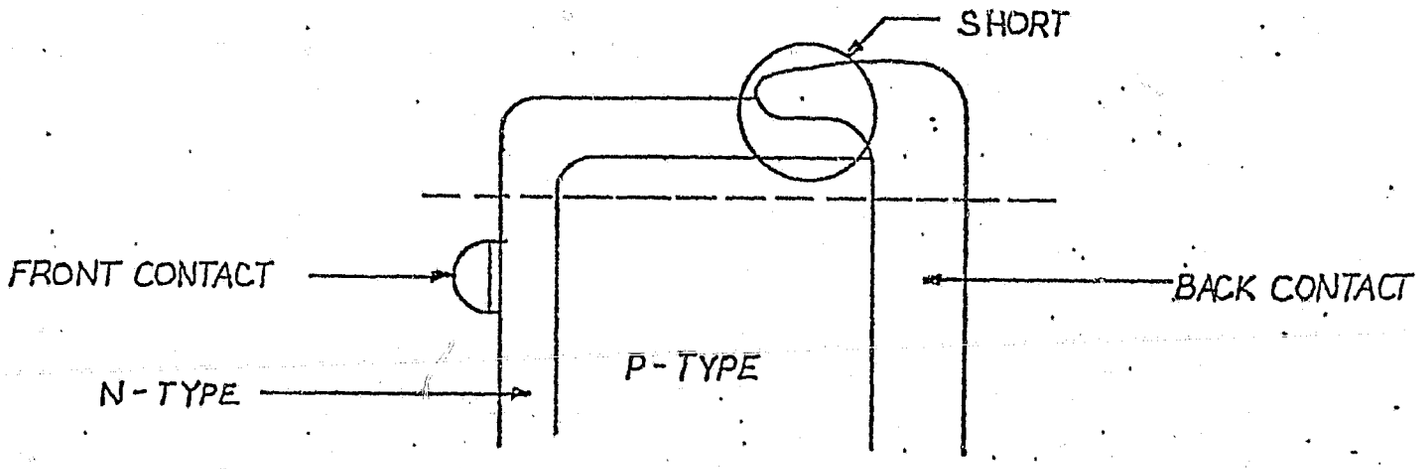


Figure 5.2 (Not to scale)

Edge removal can be carried out by means of an etching process. We propose to use automated equipment to load wafers on a vacuum chuck and spin while an abrasive tool grinds off the necessary cell material. The operation can be done at a rate of about one wafer per second. Verification work is not required due to previous experience with this process at Solarex. Adaptation to an automated environment is considered very high without foreseeable barriers. The process uses a negligible amount of abrasive material, making it highly cost effective.

The final step in the metallization process is solder coating of the cells. Solder is used to increase line thickness and thereby improving conduction of current. The process consists of moving the solar cell through a standing wave of solder in a wave solder machine. The solder will only adhere to the nickel plated fingers and back contact, leaving the bare silicon exposed.

The procedure for correct solder dipping consists of first passing the wafer through a flux solution and drying it. The melted solder is held approximately 262°C which is 38°C above liquidus. The wafers are slowly dipped into the flowing solder bath and removed quickly to avoid excessive nickel sintering. The solder composition found to be most effective consisted of 63% tin and 37% lead at 262°C ± 4.5°C. The cells have domonstrated acute line definition with consistently even surfaces on the front and back contacts.

In order to produce evenly coated surfaces and provide good electrical conductivity, various parameters should be controlled. The temperature at which the solder is held or its wetness property is important to proper coating of the cell. In addition, the solder must be constantly circulated in order to inhibit oxide formation on the surface of the solder bath. A wave solder machine will circulate the solder from the bottom to the top through a central tube. It is into this tube that the cells are dipped assuring a clean coating process.

5.1 Verification of Metallization

A large amount of work has been performed on the verification of the proposed metallization technique. The critical parameters of each substep have been carefully reviewed and a series of verification experiments has been designed for each. The result of this work is presented in this section.

5.1.1 Silk Printing

Silk printing technology is well known throughout the semiconductor industry and therefore has required little adaptation for coating solar cells. Polyurethane varnish combined with titanium dioxide powder has been identified as a good ink for negative silk printing. It is the only substance tried which yielded good line definition and adequate resistance to the nickel bath. The thixotropic nature of the resist works well with large screen sizes in the order of 100 squares per inch. In addition, polyurethane holds up to the nickel plating solution yet is easily removed with organic solvents. Work with different mask designs has shown that simpler patterns and thicker lines yield a much greater percentage of reproducibility. Either polyester or stainless steel screens are adequate to produce the line resolution necessary. It has been found that the stainless steel screens are more durable for automation, but the polyester is more readily available for experimentation.

5.1.2 Electroless Nickel Plating

When the wafers emerge from the electroless nickel plating solution, they must be sintered to assure permanent contact adhesion. Experiments have been conducted in which the solid state diffusion of nickel into silicon has been measured to determine that point at which adhesion is assured. Nickel creates electronic states deep within the bandgap that enhance recombination. If such electronic states become prevalent within the junction region, cell performance is degraded. On the other hand, it is advantageous to create such states in the silicon immediately adjacent to the metal contacts to prevent a Schottky barrier that lowers the photovoltage.

The typical chemical reaction of electroless nickel plating is:

$$2H_2PO_2^- + 2H_2O + Ni^{++} \rightarrow Ni + H_2 + 2H^+ + 2H_2PO_3^-$$

The main reaction caused by the reducing agent is a hydride ion formed by catalytic decomposition of the hypophosphite ion. Additional chemicals are added to enhance nickel adhesion, and to increase plating speeds. The most effective plating solution found is produced by J. E. Halma Company (#139-50011-71) in which the temperature and pH are self-regulating. A pH of 8.0 - 8.2 is reached through the addition of ammonium hydroxide and a proper temperature of about 90°C must be maintained so as to minimize evaporation of the ammonia.

In view of the advantages of nickel sintering; 1) elimination of the Schottky barrier, and 2) adhesion enhancement, the parameters that govern successful plating must be determined. Diffusion can be effectively regulated by temperature and exposure time. The objective is to determine the sintering time and temperature at which the nickel will firmly adhere to the silicon but not diffuse to the junction depth.

A series of experiments have been performed to quantify the diffusion rate of nickel into silicon. The reverse leakage current at 300 mV on an unilluminated 2cm x 2cm cell was used as a measure of nickel's effect on the junction. The wafers were coated entirely in an electroless nickel bath and then were alternately sintered and measured using several sintering temperatures. This technique can measure effects that would barely be noticed with light measurements.

The results of the sintering experiments performed at Solarex are summarized in Figure 5.1.2.1. Nickel diffusion becomes moderately paced around 350°C. At this temperature the forward leakage current increases by a factor of about three after three minutes indicating that cell performance has been degraded by about 30%. It can also be seen that at lower temperatures (200°C - 300°C) the forward leakage current reaches what seems to be a plateau

NICKEL SINTERING

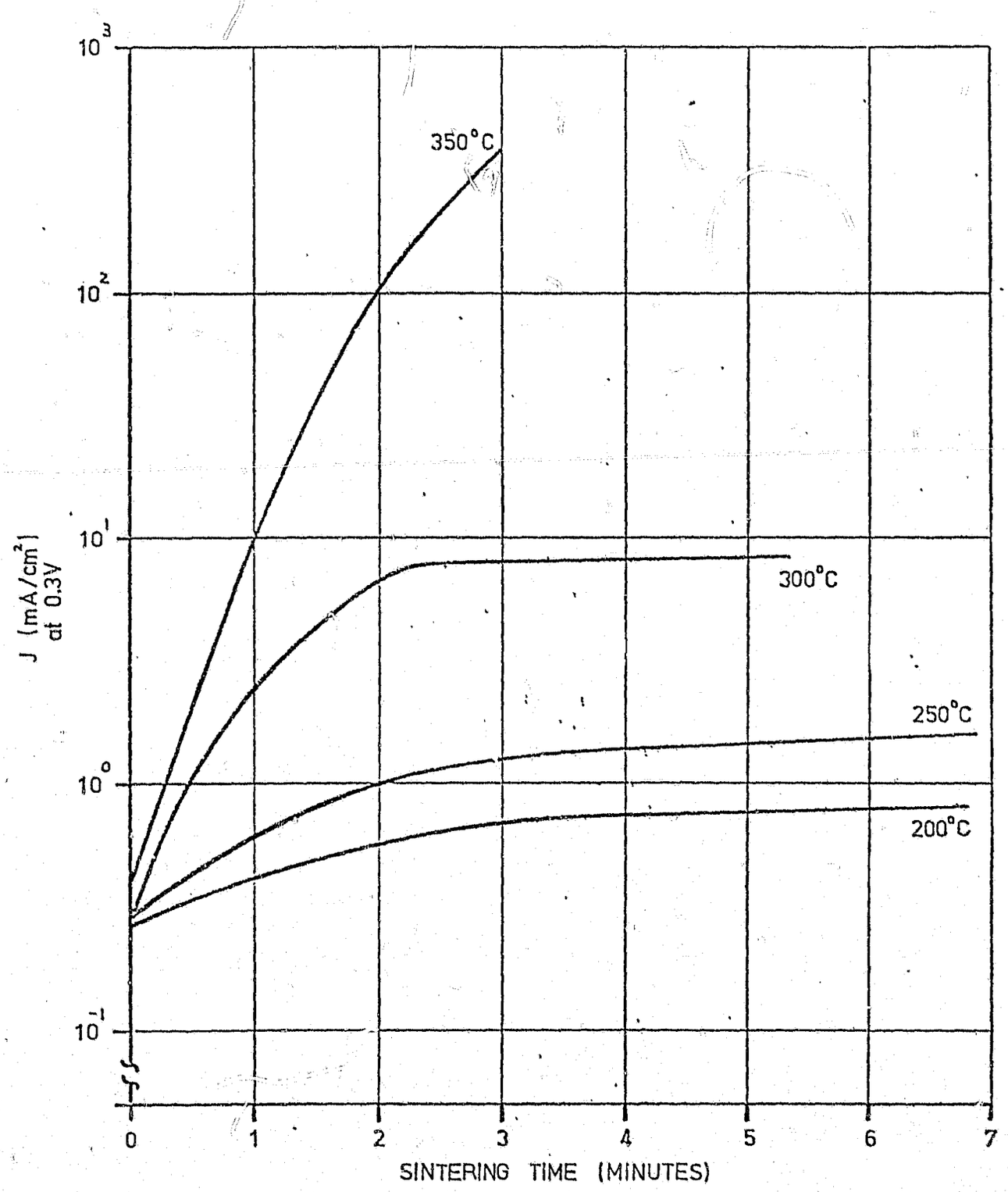


Figure 5.1.2.1

where no further damage to the junction is done. This is most apparent when we sintered close to the solder dipping temperature of 250°C with little observable deleterious effect even after two hours of exposure. This seems to be the highest temperature that will not significantly affect the cell. At 250°C the leakage current is about 1 mA/cm^3 which corresponds to a 3 to 5% degradation. Figure 5.1.2.2 displays a semi-log plot of the activation energy of the leakage current taken after two minutes. The activation energy of 1.3eV indicates that at high temperatures the forward leakage current will increase very rapidly, whereas, at the lower temperatures the graph tends to level out.

The silicon/nickel interface has also been studied optically. This was done in order to determine what method of diffusion occurs such as spiking or motion along dislocations, for example. Small sections of solar cells were embedded in plastic and sectioned at 3° from the surface plane. In this way, shallow features can be stretched so that a depth of one micrometer appears on the surface with a width of 19 micrometers. Pictures were taken of the samples at three magnifications shown in Figures 5.1.2.3, 5.1.2.4, and 5.1.2.5. Due to the low magnifications of these pictures (118X) we were not expecting to see the nickel diffusing through the junction. The pictures did

SEMI-LOG PLOT OF ACTIVATION ENERGY

(@ 2 min.)

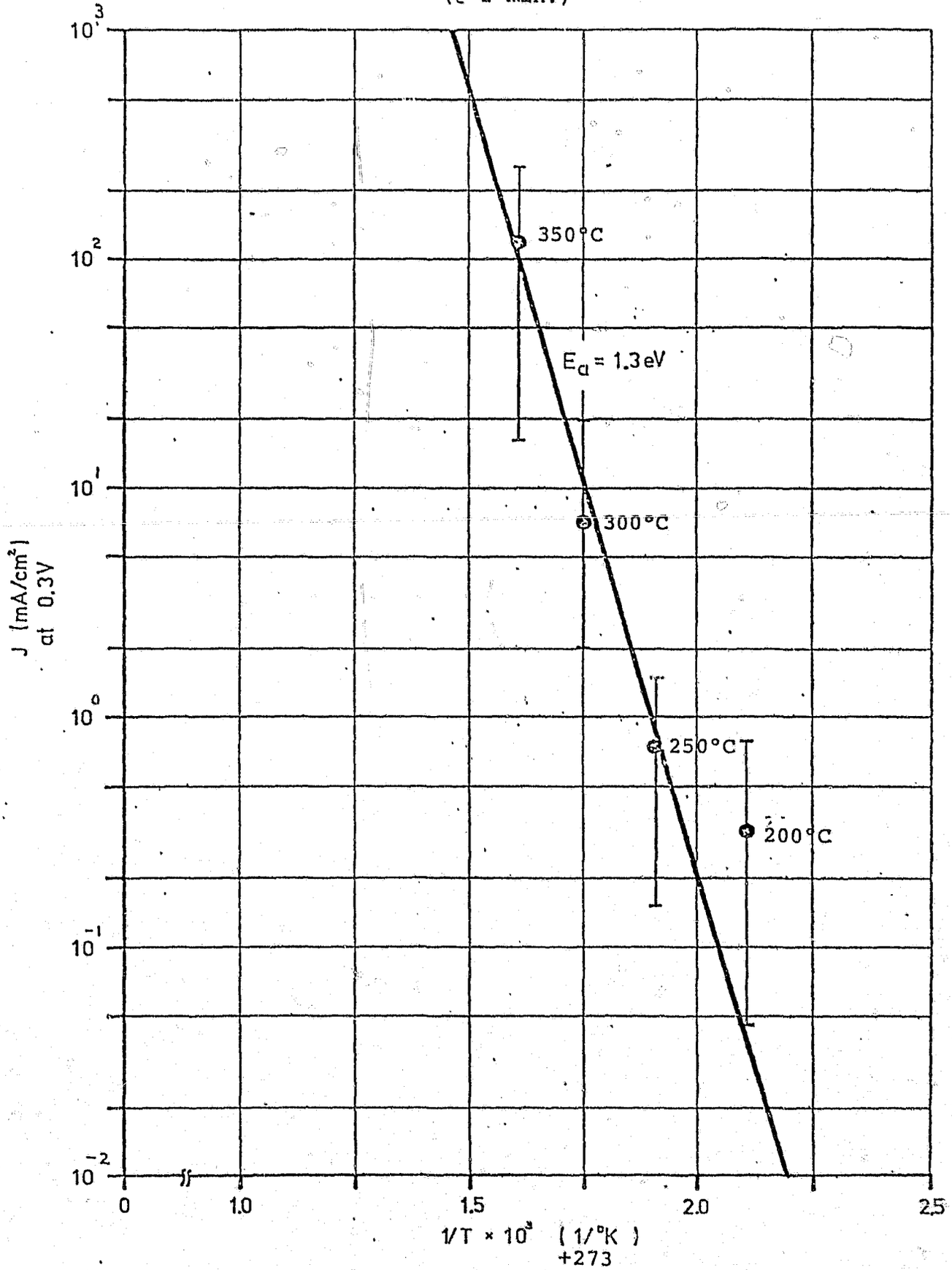


Figure 5.1.2.2

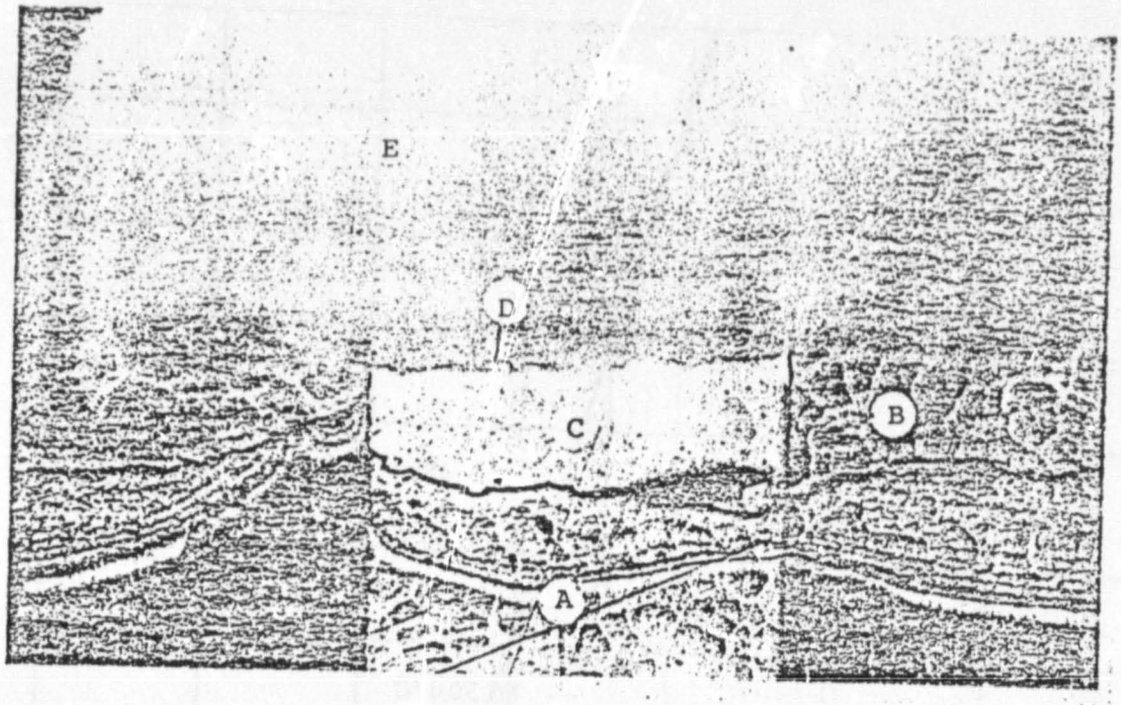


Figure 5.1.2.3

Nickel Contact Sintered at 350°C, 1 minute, 30X

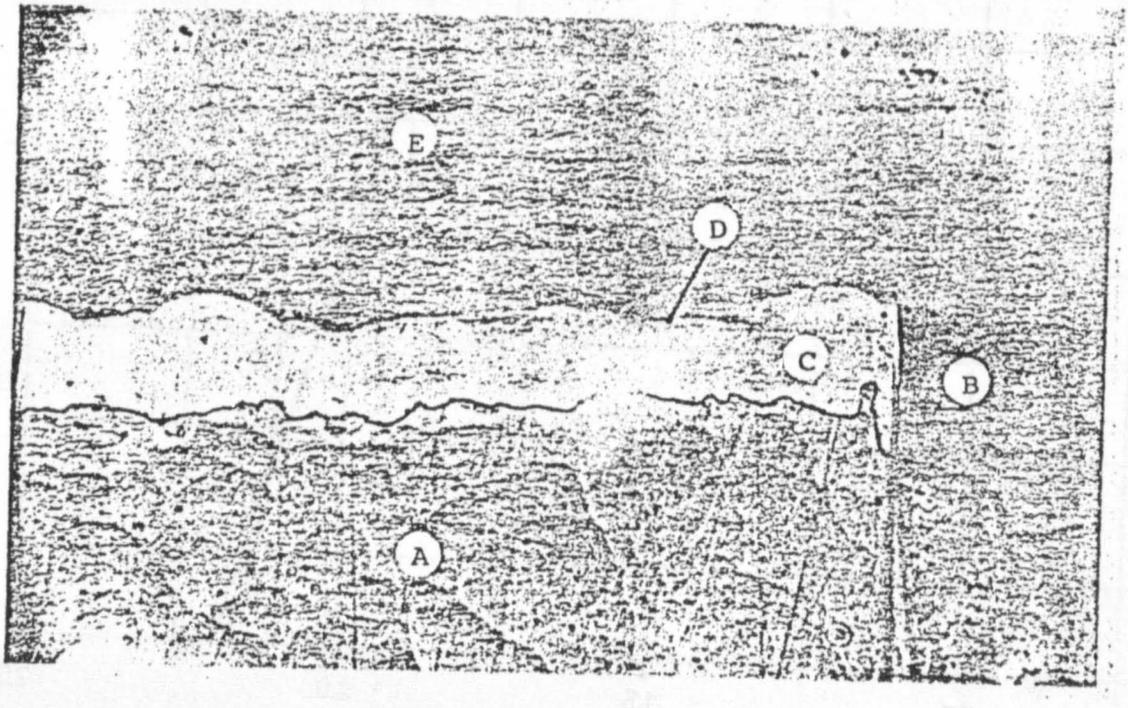


Figure 5.1.2.4

Nickel Contact Sintered at 350°C, 1 minute, 59X

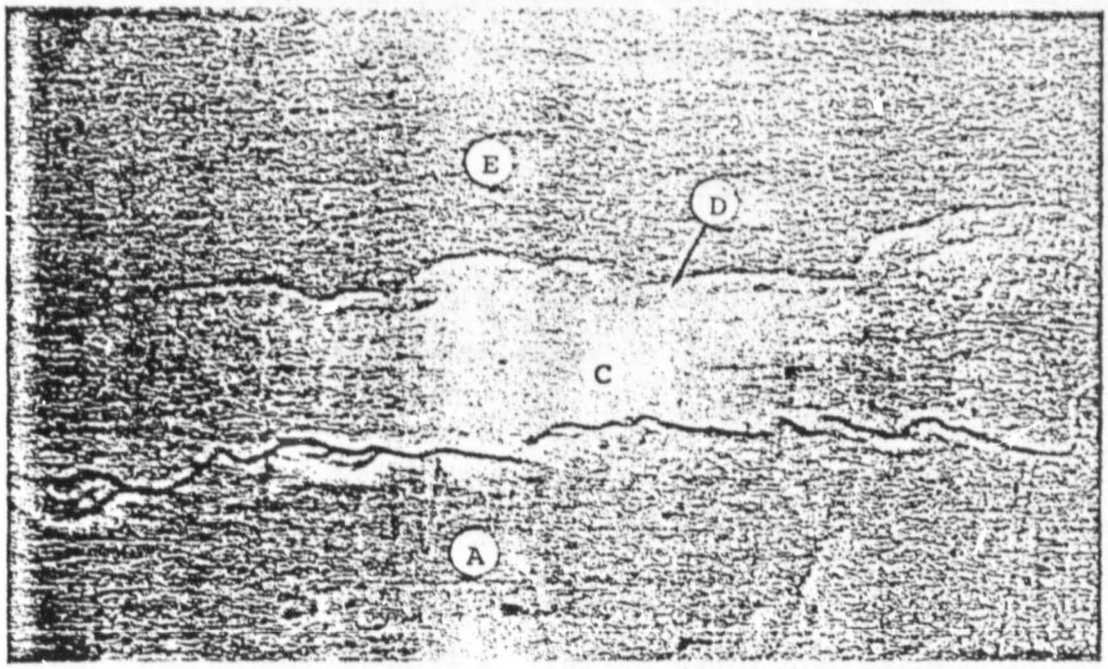


Figure 5.1.2.5

Nickel Sintered at 350°C, 1 minute, 118X

Key to regions in pictures

a) Plastic used for imbedding sample

b) Silicon surface exposed through torn plastic. ("pillowed" by alkaline etch)

c) Nickel surface

d) Angle lapped nickel

e) Angle lapped silicon

reveal that there was no spiking although the exact method of diffusion is not readily apparent.

5.1.3 Contact Adhesion

Even though the process of metallizing solar cells in an automated fashion has been successfully developed it is necessary to study the contact strength of the metal to silicon interface. A solar panel experiences stresses caused by temperature variation and mechanical loading due to wind forces. It is essential, therefore, that the metallized contacts have enough strength to withstand these forces. For this reason pull strength tests have been developed to accurately measure and study the adhesion properties of the contacts. This section will present the results of tests performed at Solarex and their significance to panel lifetime.

Table 5.1.3.1 presents the results of pull strength tests performed in accordance with the Air Force specifications for space cells (MIL-C-83443A). The specifications state that at a 45° pull angle the minimum passing requirement is 250 grams. It can be seen from the table that the mean strength obtained for our cells (1163 grams) exceeds the Air Force standards by about a factor of five.

PULL STRENGTH OF WAVE SOLDERED CELLS

AT 45°

SAMPLE #	PULL STRENGTH (grams)
1	1274
2	1415
3	1387
4	1415
5	905
6	1415
7	1174
8	1104
9	849
10	1330
11	849
12	1132
13	1302
14	1358
15	905
16	1188
17	1132
18	1358
19	1018
20	933
21	1387
22	1245
23	679
24	1019
25	1302

MEAN PULL STRENGTH:

1163 grams

TABLE 5.1.3.1

Another set of pull strength tests (Table 5.1.3.2) was performed in which the tabs were pulled at 90°. This pull angle conforms to the JPL specification for flat plate panels. The mean pull strength of these cells, 285 grams, easily satisfies the 225 gram JPL passing requirement.

The joint failure for both sets of tests was most often the silicon itself and not the metal to metal interface nor the metal to silicon interface. In the proposed three-step metallization process there are two interfaces formed, the silicon/nickel and the nickel/solder. The failure of tabs pulled occurred deep within the silicon forming craters in the surface. This, once again, demonstrates the excellent adhesion properties achieved with this technique.

In addition to the pull strength tests, the cells were subjected to humidity tests. The tests lasted one month at 90% relative humidity and at 72°C. The cells were tested every few days; no degradation was detected over the entire duration of the test.

All of the tests performed on contact adhesion clearly indicated that our proposed metallization technique can withstand harsh environmental conditions.

PULL STRENGTH AT 90°

SAMPLE #	WAVE SOLDERED (grams)	SAMPLE #	VACUUM (grams) METALLIZATION (Ti-Ag)
12	799	1	317
8	397	2	340
88	170	3	416
10	227	4	408
15	198	5	262
14	17	6	378
13	85	7	316
25	284	8	338
19	510	9	354
20	255	10	370
24	198	11	374

MEAN PULL STRENGTH	MEAN PULL STRENGTH
285	352

TABLE 5.1.3.2

5.1.4 Sheet Resistance and Shadowing

There are three major, unavoidable sources of power loss that are influenced by the metallization geometry. These are:

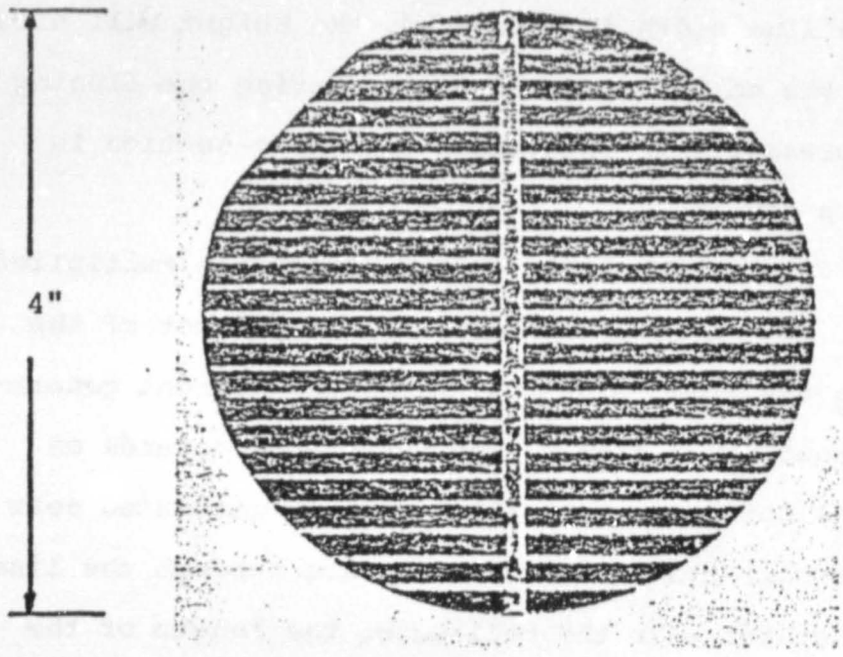
1) the voltage drop across the conducting lines of the pattern,
2) the voltage drop across the thin diffused region, and
3) shadowing, since the metal lines are opaque

These losses are inherent in any solar cell configuration and none can be eliminated without increasing the others.

Using a simple pattern, as shown in Figure 5.1.4.1 a mathematical equation for power loss due to metal coverage can be derived. From the equations the ideal line width and spacing between lines can be derived. This in turn indicates the printing resolution required and the amount of power loss that is unavoidable.

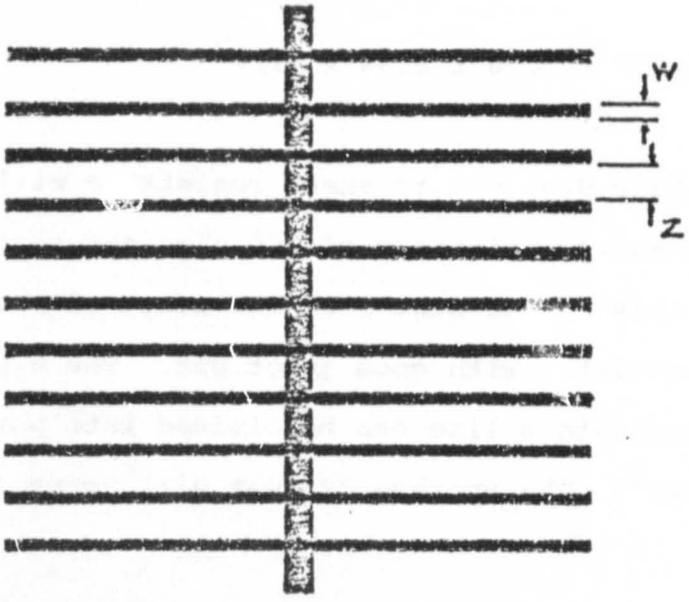
The calculations are based on a 10.16 cm (4 inch) diameter cell with a central buss and a uniform set of lines perpendicular to the central buss. The central buss will be fixed at a width of 2 mm., which gives 2% shadowing and a negligible series resistance. The variables will be the line width, w, and the distance between lines, z, (see Figure 5.1.4.2).

The voltage drop due to line resistance can be calculated using the formula $R = \rho \frac{L}{A}$. The resistance, R, is the product of the solder resistivity, ρ, (15×10^{-6} Ω-cm) times the length of the current path, L divided by the cross sectional



Textured, Wave Soldered Solar Cell

Figure 5.1.4.1



Metallization Pattern

Figure 5.1.4.2

area, A. If the line width is increased, the height will also increase due to the solder meniscus formed during the dipping process. To represent this phenomenon the cross-section is approximated by a square.

The voltage drop in the line, is the resistance multiplied by the current. The current, in turn, is the product of the area surrounding the line, 5.08 x z, times the current generation density, about 0.032 A/cm^2. The resistance depends on the length of the current path. Since current generated near the central buss will flow a shorter distance through the line than current generated near the cell edge, the length of the current path is not a fixed number. To a good approximation, however, the line length can be taken as a final number, 2.54cm, the distance from the central buss to the midpoint. From the above considerations we can write the equation for voltage drop in the line, calling it VL, as follows.

$$VL = (0.032 \times 5.08 \times 2.54 \times z)/w^2$$

The voltage drop due to sheet resistance will now be derived. A sheet resistance of 100 ohms per square will be used since this is the center of the range of sheet resistance that is correlated with good junctions. The area from which current flows into a line can be divided into parallel squares of area $(z/2)^2$. The average current will actually travel

half the length of the square so the resistance will be taken as 50 ohms. The voltage drop in the diffused sheet, called VS, can be written as:

$$VS = (R_{sheet}/2)\ (0.032)\ (z/2)^2$$

The fractional power loss due to both voltage drops can, therefore be written as:

$$(VL + VS)/0.45$$

where 450 mV is the usual operating voltage at the peak power point.

The current reduction resulting from shadowing by the perpendicular lines can be written as w/z. This assumes that the initial efficiency includes the central buss shadowing.

Figure 5.1.4.3 is based on a sheet resistance of 100 ohms per square, the center of the range of the sheet resistance that is correlated with good junctions. It can be seen from this graph the best possible final efficiency is 13.4%. The immediate question is whether it would be worth generating a lower sheet resistance in order to reduce the number of lines per centimeter. Figure 5.1.4.4 based on 50 ohms per square, indicates that a slight improvement can be obtained. Another trade-off occurs in deciding between the line width and the

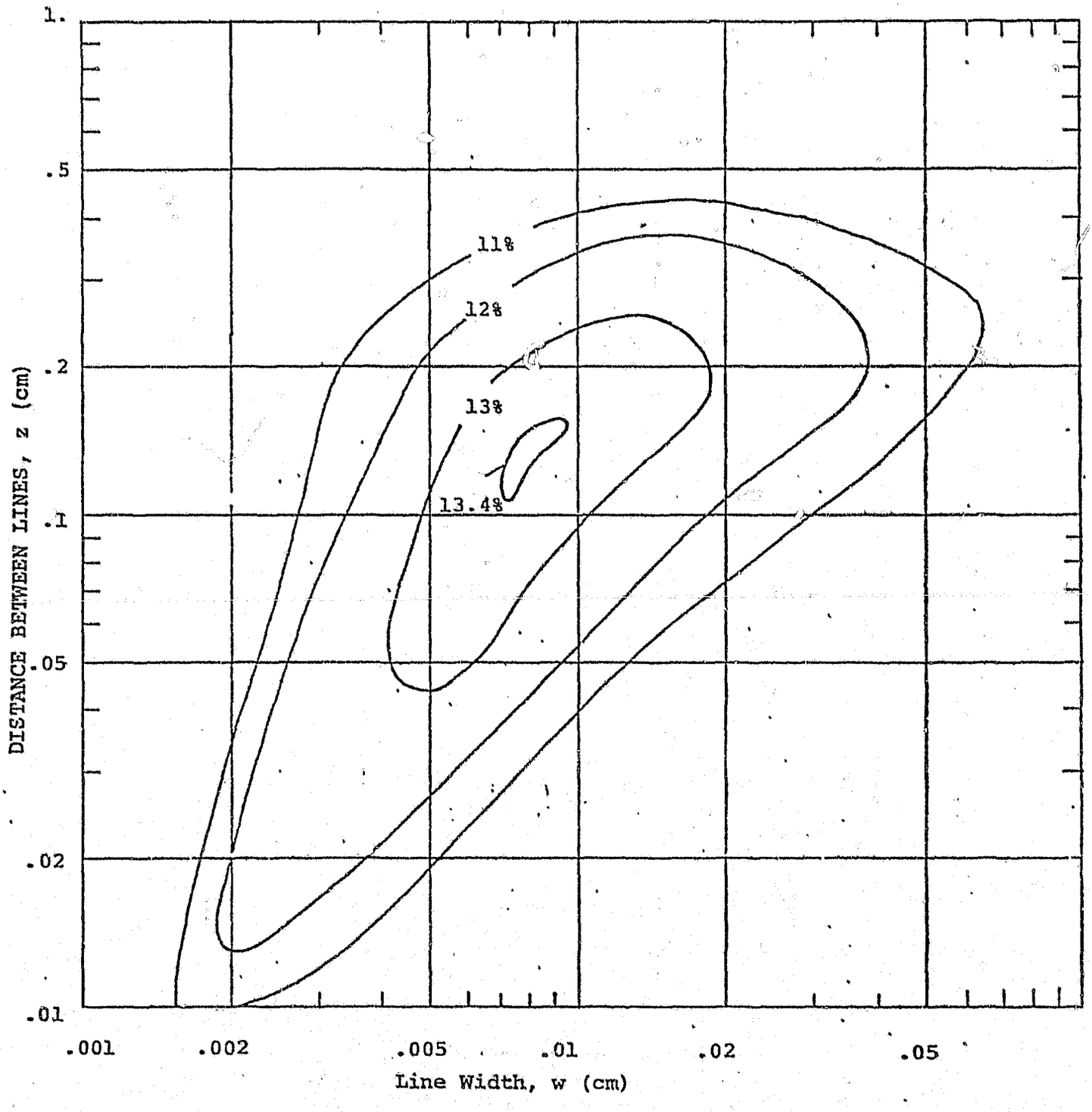


FIGURE 5.1.4.3 EFFICIENCY, 100 Ω/□ SHEET RESISTANCE

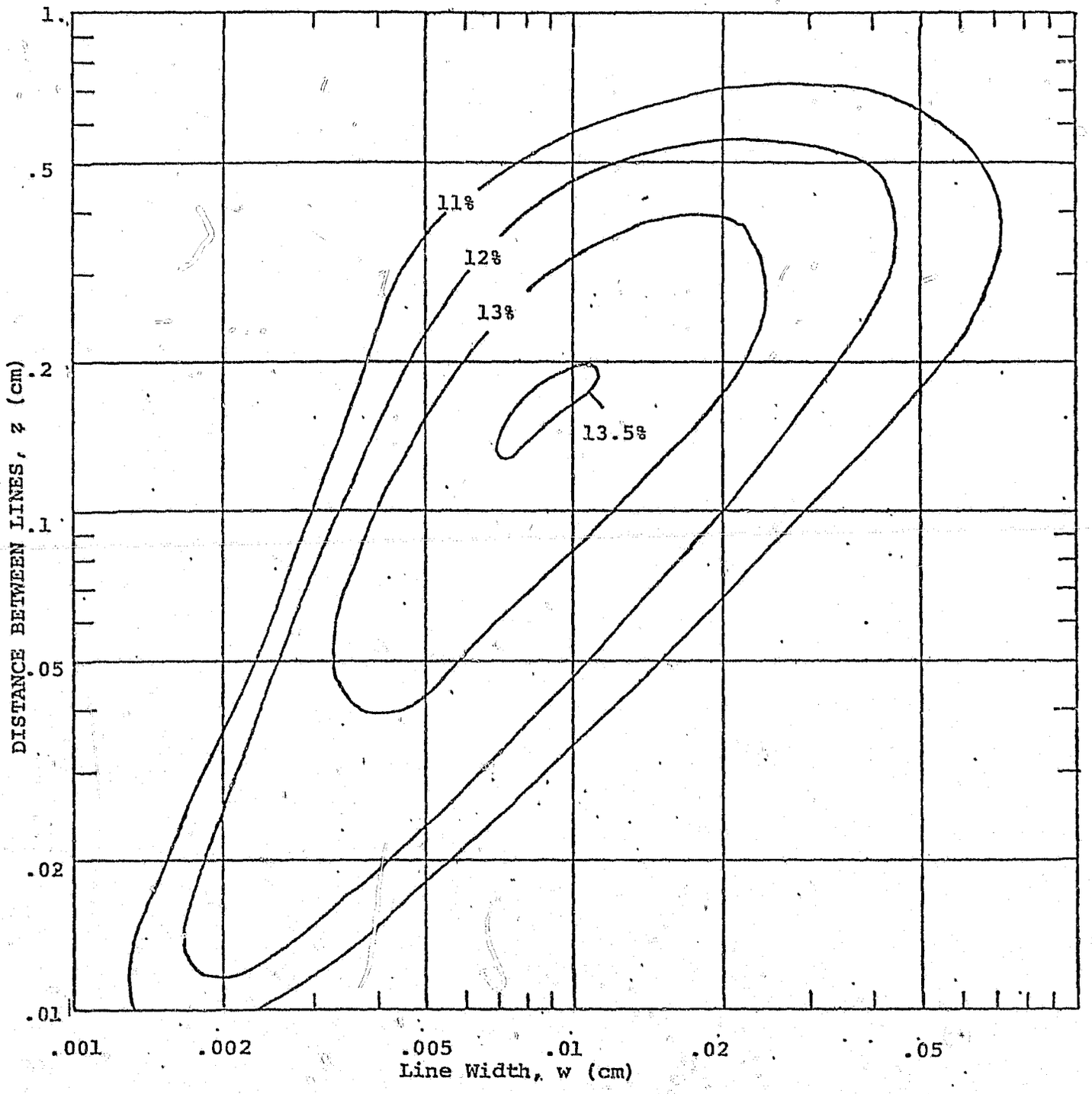


FIGURE 5.1.4.4 EFFICIENCY 50Ω/□ SHEET RESISTANCE

desired cell efficiency by 0.5%, line width can be increased by 0.01cm (3.9 mils). Wider lines are desirable for greater contact adhesion and ease of silk screening. In any case, the computer indicated that the ideal line width, for 100 Ω/□ sheet resistance, is about 0.0027" - 0.0035". For 50 Ω/□ sheet resistance lines should be as wide as 0.0094" to obtain 13% efficiency. In either situation the resolution indicated is achievable with screen printing.

6. Testing

The completed cells must be tested with respect to front contact adhesion and electrical characteristics. An automatic cell testing machine can be envisioned which performs these two tests at a rate of 120 wafers per minute. Mechanical testing assures that the metal fingers of the cell adhere firmly and make ohmic contact with the silicon. Electrical testing determines the quality of the cell and also provides important information on the individual process steps during cell manufacture. The diode curve, for example, is a sum of exponential factors that indicate the quality of the bulk silicon, the defect density at the junction, and the recombination velocity of the charge carriers at the surface edge. These are all factors which directly relate to variations in parameters in the process steps of cell production.

The testing procedure can be performed automatically with the aid of a minicomputer. The front contact pattern can serve as a guide to a laser scanner or CCD optical matrix to align the cell on a metallic plate for testing. Adhesion will be checked by brushing with a camel hair brush on the front surface of the cell. The remaining contact pattern can be identified by means of optical character recognition technology, similar to the one currently employed in supermarket checkouts using the uniform product code (UPC). Cells with a certain percentage of front fingers missing will be ejected. Electrical testing can be performed by utilizing the metallic plate to contact the cell

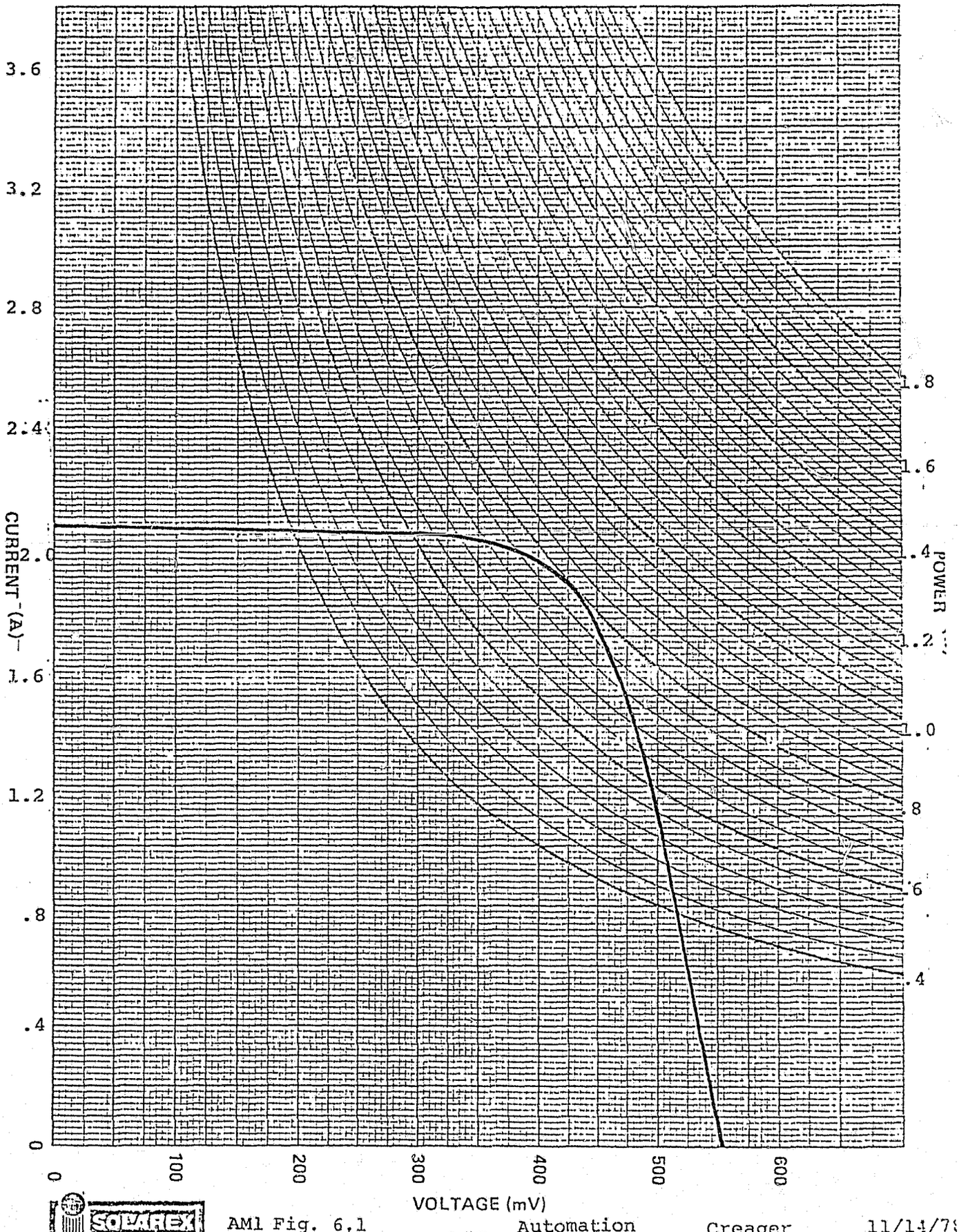
back and by lowering an electrode onto the front surface near the cell edge. The cell will be illuminated with controlled intensity and a computer driven variable power supply will measure its electrical response on an IV curve. Continual calibration procedures can be made an integral part of the computer program. Depending upon the cell's performance with respect to a preset value, it will be passed or removed from the production line.

The automation of egg handling and mechanical watch assembly are examples which demonstrate that there are no physical limitations to testing delicate materials at a rate of 120 wafers per minute.

In a similar manner, machines can be developed to handle and test solar cells. Precise positioning and delicate application of contacting force are important factors which can be adjusted to insure accurate testing with a minimum of breakage.

Current vs. voltage curves were plotted for a cross section of solar cells produced under this contract. Over fifty cells were selected ranging from the first batch to the last batch of cells produced. A sample curve from the last batch is presented in Figure 6.1 which shows an 9.8 efficiency cell (800 mW). The cells tested ranged from 570 mW to 810 mW (7% to 10% efficient), and the short circuit current and open circuit voltage remained constant at about 2.1A and 550 mW respectively.

VOLTAGE CURRENT CHARACTERISTICS OF 4" TEXTURED CELL



SOLAREX ROCKVILLE, MARYLAND USA

AM1 Fig. 6,1

Cell Type Automation By Creager Date 11/14/7

These favorable results indicate that the potential for realizing the LSA project goals is very high. Cells producing the stated efficiencies are an excellent base material for module fabrication.

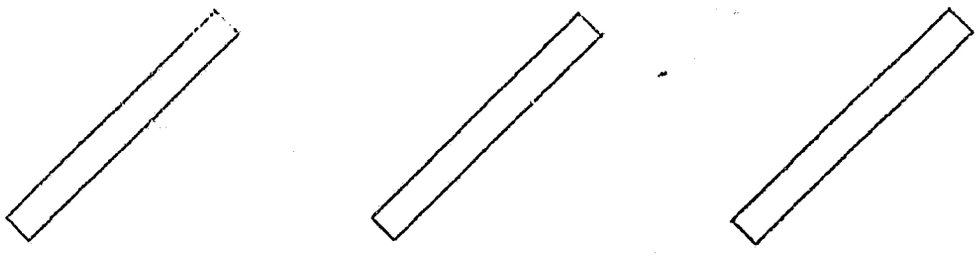
7. Interconnection and Encapsulation

The final phase of the automated assembly involves the fabrication of solar modules in a cost effective manner. In order to produce arrays which will withstand all environmental conditions, careful selection of process sequences and materials is required. Over its expected 20 year lifetime the panel will be subjected to varying temperature cycles, humidity, and rain, as well as hail and wind forces. Throughout all of these conditions the cells must be kept totally isolated from moisture, yet remain flexible enough to allow for thermal expansions. In addition, the system of interconnection and encapsulation should readily interface with automated machinery. This section will describe the process which we believe to have great potential.

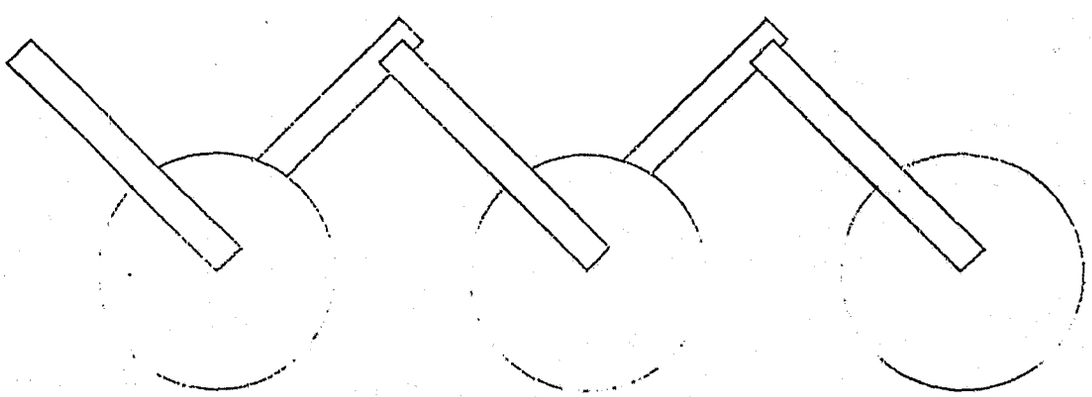
In order to meet its many requirements, the proper selection of superstrate must be an inexpensive material that endures environmental conditions for years while retaining high transmission properties. We have chosen glass as the superstrate because it is an abundant material which serves both as an encapsulant and as a structural support. In addition, it remains clear and can be easily cleaned.

The laminating materials were selected from a wide variety of candidates. An acrylic resin is used to secure the cells and allows solder reflow for interconnection purposes. A polyester back sheet will seal off the panel efficiency due to its reflective properties. These materials were selected because they showed great promise of meeting these laminating requirements.

The proposed panel building process begins by preparing the superstrate, typically a 4' x 2' sheet of glass. The glass is ultra cleaned by immersing it in a weak hydrofluoric acid bath. As part of the interconnection scheme, tabs are applied directly on the glass by means of an arc-sprayer. The technique involves spraying two metals consecutively through a mask onto the glass. Aluminum is sprayed first because of its excellent adhesion properties to glass. Then copper is sprayed exactly over the aluminum to aid in the electrical conduction of the tab, and to make it solderable. Finally, the tab is tinned with solder in preparation for the solder reflow step. In the meantime, cells coming from the testing station are tabbed with strips of tabbing material on the back at a particular angle. This is done so that the cells which are positioned on the glass will all be mechanically interconnected as shown in Figure 7.1. Both the glass and the face of the cell are primed with an acrylic spray to ensure adhesion. The acrylic laminate is applied and spread evenly over the surface of the glass. Before the panel can be assembled, however, the solvents in the acrylic resin must be driven out. This is accomplished by a process we refer to as outgassing, whereby the acrylic coated glass is subjected to 170°C in an oven. The cells are then positioned face down on the glass, so that the main buss bar of the cell covers half of the arc-sprayed tab on the glass. A white polyester sheet is laid over the back of the panel and the



Arc Sprayed Contact Pattern On Glass, Enforced by Solder



Cells Positioned Face Down With Their Back Contact Tab Overlapping the Front Contact Pattern of Adjacent Cell. (Simplest conceptual arrangement)

Figure 7.1

whole system is pressed together and heated simultaneously. The solder on the cell and arc-sprayed tab will reflow and connect to one another, as will the tabbing material on the back of the cell and the arc-sprayed tab. In addition, any excess acrylic under the cell will flow towards the edge and seal off any gaps formed between the polyester/cell/glass interface. Therefore, by pressing and heating the components together, the panel will be interconnected and sealed off in one step.

7.1 Verification

Verification work on this process has been divided into three major sections; 1) arc-spraying, 2) lamination and 3) solder reflow. These will be discussed according to the order in which they occur in the process.

7.1.1 Arc-Spraying

Arc-spraying tabs on glass was selected as part of the interconnection scheme because of its simplicity and adaptability to automation. By arc-spraying tabs on glass, one-half of the hand operation of tabbing can be eliminated, which results in large cost savings. The process also has a high rate of reproducibility, yielding consistent patterns from one glass sheet to another.

An arc-sprayer produces an electric arc between two electrodes through which metal wires are fed towards each other. The molten metal from the wires is sprayed forward with a high velocity. The heat and force of the spray depends on the distance between the nozzle and the receiving material, as well as the air pressure and arc-current.

Table 7.1.1.1 summarizes the results of spraying different metals.

Material	Solderable?	Adhesion to Glass
Aluminum	No	Excellent
Low Carbon Steel	No	Excellent
Aluminum/Bronze	No	Peels off with hard pressure
Nickel/Aluminum	No	Peels off with hard pressure
Copper	Yes	Peels off with moderate pressure
Phosphor Bronze	Yes	Peels off with hard pressure.

TABLE 7.1.1.1

As mentioned earlier, the aluminum exhibited excellent adhesion properties on glass. It is believed that a chemical reaction

occurs between the glass, whose major constituent is silicon dioxide, and the aluminum, which bonds readily to oxygen. Also, aluminum melts at the softening point of glass (~660°C).

Copper, on the other hand, did not adhere to glass yet solder wets to it readily. This three metal tab was, therefore, developed to satisfy all of our parameters. In sum, aluminum adheres to glass, copper adheres to aluminum, and solder wets copper. This provides excellent adhesion and conductivity properties.

The adhesion of the tab was pull-tested by soldering tabbing material to it and then pulling at a 45° angle. All of the tabs were pulled away from the glass at about 200 grams force or higher, leaving conchoidal fractures in the glass as can be seen in Figure 7.1.1.1 and 7.1.1.2. Care must be taken, however, in the spraying process, to ensure a strong interface. The copper must be sprayed lightly on the aluminum so that the difference in thermal expansion between the two metals will not cause warping of the tab off the glass. By adjusting the wire feed valve of the spray lead to a minimun setting, and spraying for only 2 to 3 seconds, the arc-sprayed tab will exhibit good adhesion properties.

In summary, arc-spraying has been demonstrated as a quick and reliable method of adhering tabs onto glass. This allows the interconnection step to be integrated with the encapsulation step, with considerable savings in time and an assurance of uniformity.

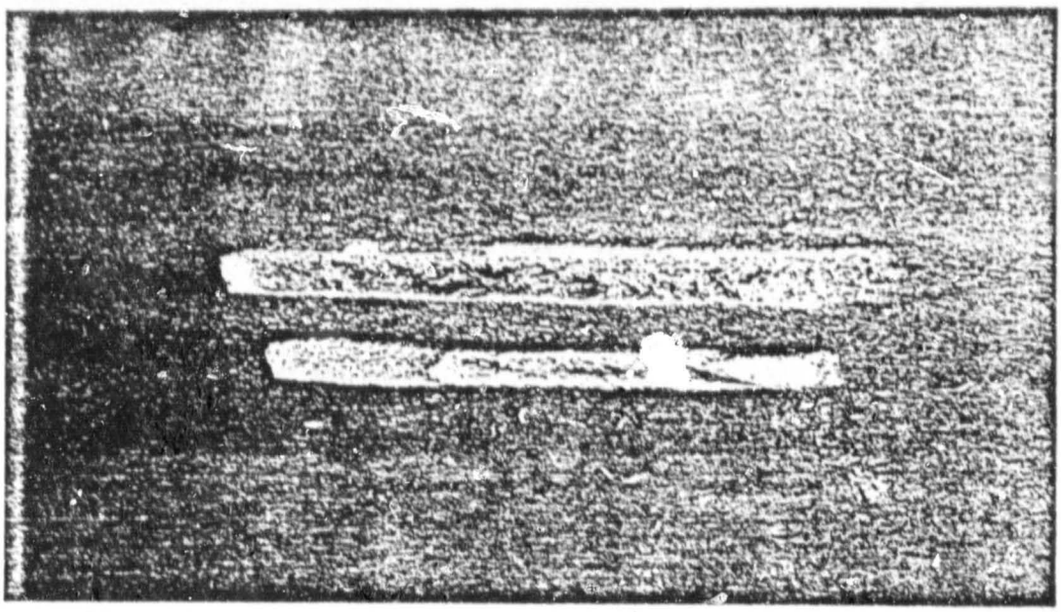


FIGURE 7.1.1.1

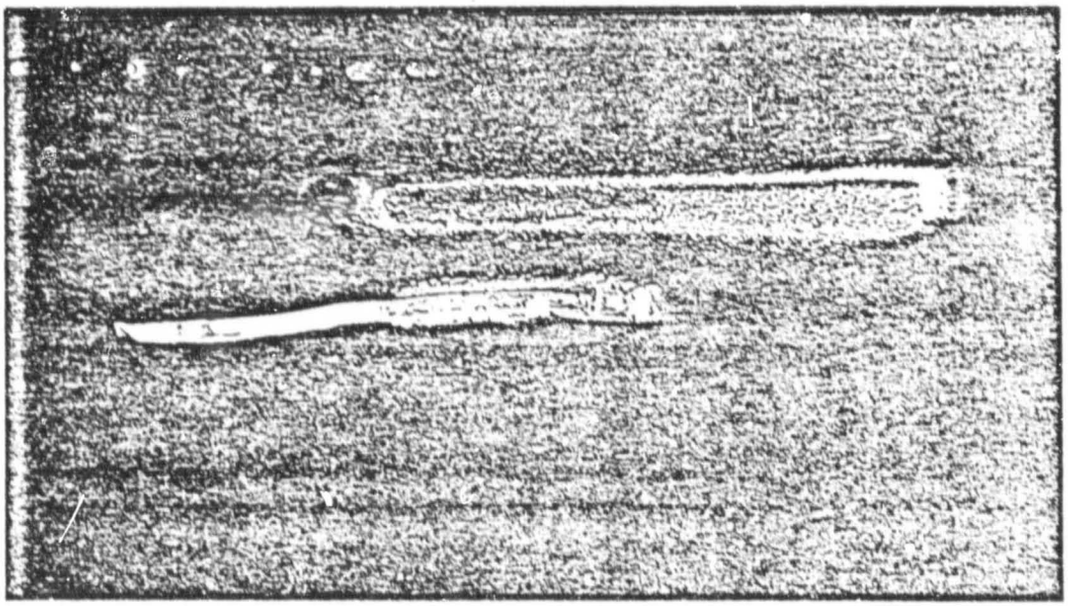


FIGURE 7.1.1.2

7.1.2 Laminating

A layer of clear plastic is applied between the cell and glass in order to assure good optical coupling and good adhesion, yet allow enough flexibility to absorb stress generated by different temperature expansion rates between the cell and the glass. The choice of materials depends upon three parameters; 1) clarity and elasticity for the life of the panel, 2) ease of application and ability to withstand high laminating temperatures, and 3) environmental isolation. A diverse group of plastics have been tried with a variety of curing procedures and application methods. A combination of two materials are being used to provide maximum protection and cost effectiveness.

A summary of the work done on encapsulation materials and methods is presented in Table 7.1.2.1. The first layer refers to that material which is between the cell and the glass, and the second layer is considered the backing of the panel. Most of the laminating systems were cured in a similar manner; that is, the materials applied to the superstrate and cell, and pressed to approximately 5 psi. They were then baked between 140°C and 170°C for 1 to 2 hours. The only exception to this was the layer of silicone on which the laminate was applied first, then put under 10 lbs. of pressure and allowed to cure overnight. The combination of acrylic spray, acrylic resin and polyester sheets seems to have the greatest promise of satisfying our laminating requirements.

SUMMARY OF LAMINATION SYSTEMS

FIRST LAYER	SECOND LAYER	RESULTS	COMMENTS
Acrylic Spray Kleer Kote 6004	Polyester Sheet 7.5 mils thick	Good Lamination Adhesion to polyester is poor Adhesion to acrylic to glass is Excellent	Outgassing of acrylic No drifting Problem
Acrylic Spray Kleer Kote 6004	3M FEK 244 Reflective Film	Poor Lamination Adhesion is good on all surfaces Mirrored surface was discolored FEK shrunk	Outgassing of acrylic is required
Acrylic Spray/ Kleer Kote 6004	Polyester Sheet Lm100W	Poor Lamination Adhesion is excellent on all surfaces	Made panel using a cell with exceptionally uneven back
Acrylic Spray/ Acrylic Resin Acryloid B-7	Polyester Sheet Lm100W	Good Lamination Adhesion is excellent on all surfaces	Most promising combination Outgassing of acrylic is required
Polyvinyl Butyral	Polyester Sheet Lm100W	Good Lamination Adhesion to polyester is poor PVB adhesion to glass is good	The cells must be secured to avoid drifting due to flowing of PVB
Polyvinyl Butyral	Polyester Sheet 7.5 mils thick	Good Lamination Adhesion to polyester is poor PVB adhesion to glass is good	The cells must be secured to avoid drifting due to flowing of PVB
Thin Layer of Silicon	Polyester Sheet 7.5 mils thick	Good Lamination Adhesion to polyester is poor	Indefinite curing time

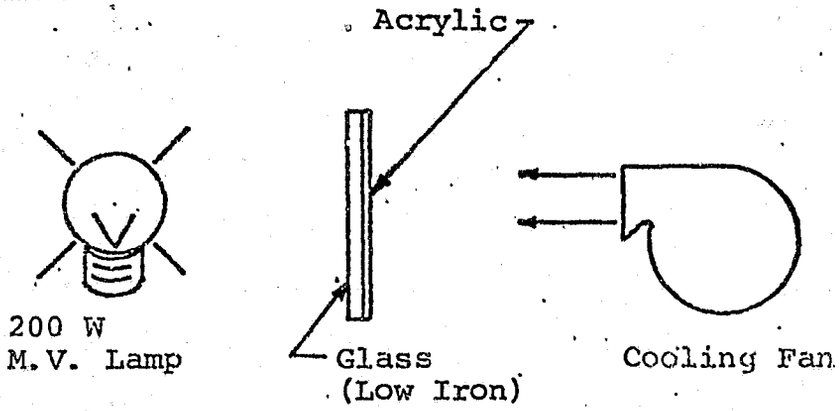
TABLE 7.1.2.1

This has been confirmed by a variety of verification experiments including corrosion studies, temperature cycling, humidity tests, and ultra-violet tests. A glass sheet with an arc-sprayed tab and the acrylic spray/resin combination was immersed in water with a heavy concentration of salt and rust for two months. After the elapsed time, the tinned arc-sprayed tab showed no signs of corrosion. It is important to note that this corrosion test was done with only the acrylic protecting the tab. It is believed that with an additional polyester backing the tab would be totally isolated from moisture, and thus the possibility of a corrosive reaction taking place would be very much reduced.

Some sample panels were also temperature cycled between -15°C and 100°C with practically no warm up or cool down time. Each panel was cycled 15 times with the time between temperature extremes varying from 1/2 minute to 2 hours. Minimum time at extreme temperatures was 2 hours, while the maximum was 3 days. None of the panels with this particular combination of encapsulants showed signs of thermal shock or discoloration. In addition, the adhesion between the glass, acrylic and polyester remained excellent. A destructive test was performed on one of the panels so that an upper bound could be determined. At 120°C small bubbles were visible between the glass and cell, and at 180°C the acrylic exhibited signs of yellowing.

The panels were humidity cycled to determine their resistance to moisture. They were kept in the humidity chamber at 90% relative humidity and 70°C for one week. Once again, no adverse effects were observed.

Finally, the panels were exposed to accelerated ultra-violet light tests. The U.V. accelerator, shown below, consists of placing a sample of glass with encapsulant 2 1/4 inches from a mercury vapor 200 watt lamp and air cooled from the back.



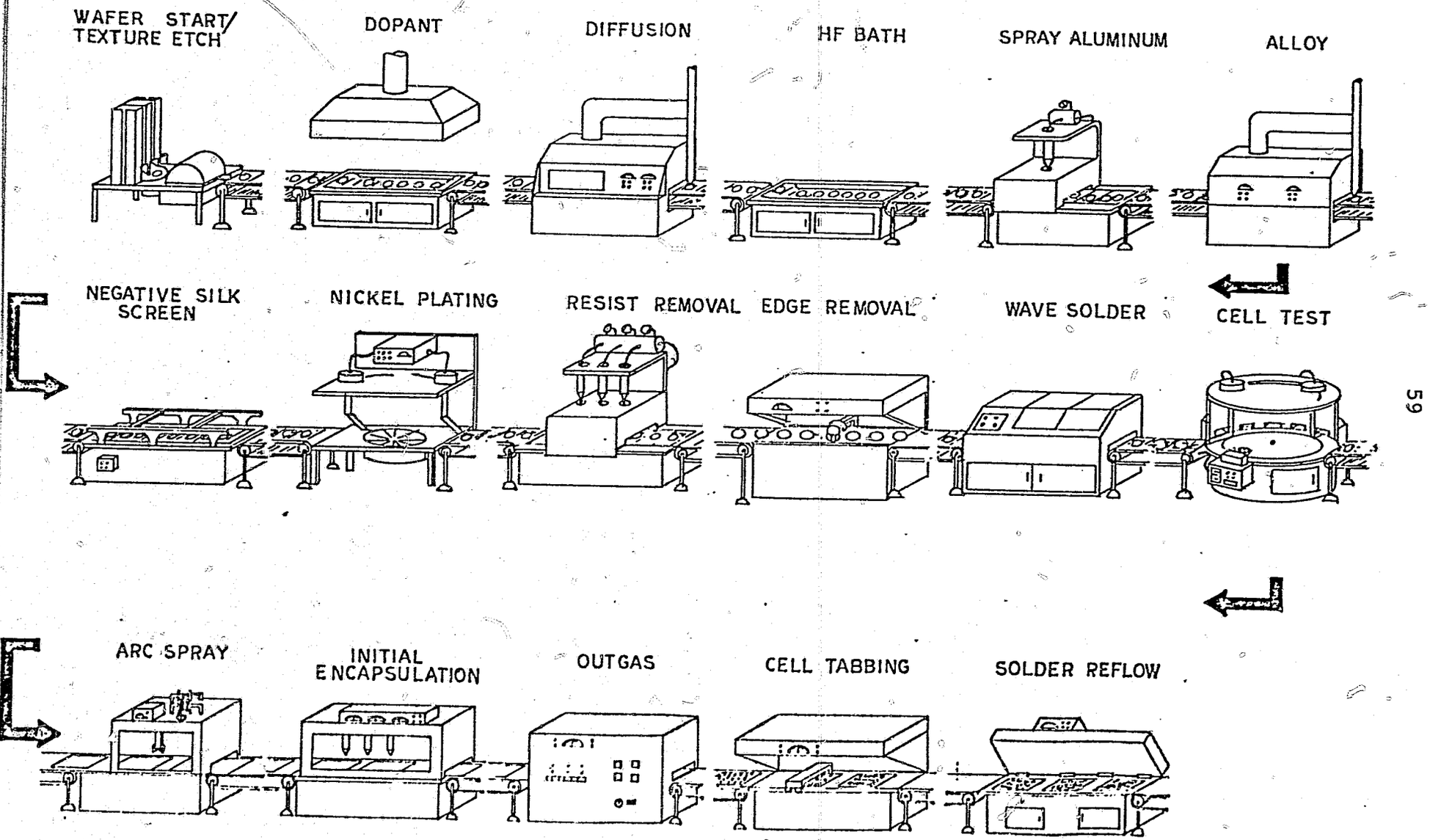
The samples survived 200 hours of constant U.V. light with little change in light transmission or appearance of the encapsulant material.

In general, the sample panels showed little or no change after being exposed to U.V. radiation, humidity, temperature cycling, and corrosion tests. We feel that this lamination sequence has great promise of effectively protecting the solar panel.

7.1.3 Solder Reflow

The last important phase of interconnection and encapsulation occurs when the modules are assembled, heated, and pressed together. The solder from the arc-sprayed tab and the solder from the main buss bar of the cell will reflow and interconnect with one another. In addition, the tabbing material on the back of the cell will connect with the reflowing solder from the other half of the arc-sprayed tab. In this way, the entire panel will be interconnected and sealed in one step. The key to this operation is in the proper selection of solder and its corresponding melting temperature. The solder should reflow at, or just above the softening temperature of the encapsulant. Since 63/37 solder is used the reflow temperature is about 185°C. If the panel is heated much above this temperature, solder from the fingers of the cell will reflow off. Another important factor is the force with which the module is pressed. A pressure of 5 psi applied incrementally has been sufficient to achieve solder reflow and interconnection between the glass and the cell.

PROCESS FLOW DIAGRAM OF PROPOSED AUTOMATION SEQUENCE



8. Economic Analysis

The principle concern of this automation contract is to produce efficient solar modules in a low cost manner. It has already been shown that the cells produced, using this process, have a great potential of efficiently converting sunlight to electricity. This section will present a cost analysis which concludes that solar modules can be produced cost efficiently for 49.75¢ per wafer. This analysis is intended to show the main cost drives in the process and not to be a rigorous accounting of every cost detail.

The cost of each process will be detailed according to material, equipment and labor estimates. The bulk silicon is assumed to cost 22¢ per wafer, the rest of material costs is based upon large volume purchase prices from respective manufacturers. The equipment cost has been estimated by two factors; first, by the cost of existing equipment and second, by the cost of fully automating that equipment. Since the process is fully automated, labor will be at a minimum.

The labor estimates are based upon the expected time of supervision and maintenance for each machine. The costs also reflect three shifts of operators per day covering twenty working hours.

All of the steps are designed to process 120 wafers per minute, which is consistent with the 50MW, a year production goal. The number and size of machines has been designed to operate at this throughput rate. It is, therefore, very important that there be a constant flow of cells through each

step. A delay in any one section can adversely affect the entire production line.

Finally, the cost analysis is based upon a price per wafer. At the conclusion of this section there will be a summary which will translate this cost into dollars per watt.

8.1 Surface Preparation

The economic evaluation of surface preparation is based upon a well known and verified technique presently used at Solarex. The cost presented for materials, represents the prices that are currently paid or are expected to be paid based on large volume.

The materials selected for this process have been specifically chosen because of their cost effectiveness and adaptability to an automated sequence. Sodium hydroxide is being used over an acid etch because of substantial cost savings and the elimination of careful handling procedures. NaOH is estimated to cost 35¢/lb. in large volume and 0.015 lb. per wafer is required. This implies a cost of 0.53¢ per wafer. Likewise, potassium hydroxide etch is an excellent method of producing a non-reflective surface as discussed in Section 2. The cost savings over the comparable AR coating is considerable when the cost of vacuum systems along with the additional handling requirements are taken into account. KOH is expected to cost 50¢/lb and 0.015 lb/wafer is needed, therefore, the materials cost can be estimated at 0.75¢ per wafer.

Automatic handling equipment for solar cell cassettes is already available. The work damage removal requires a 10 minute resident time and texturing can be accomplished in a 15 minute etch. Machinery can easily be envisioned which passes cassettes (holding 25 wafers each) through an etch bath at a rate of 120 wafers per minute. This equipment including belt transport systems, etch baths, and rinsing stations is estimated to cost $200,000 and expected to operate for 5 years. This results in a cost of 0.08¢ per wafer for all equipment.

It is expected that only one operator needs to be present to supervise the continuous flow of cassettes. Each operator will cost $20,000 a year in labor and overhead which suggests a cost of 0.12¢ per wafer. The process will be run continuously between three work shifts to fully utilize the capitol equipment.

A summary of these costs is presented in Table 8.1.1. Energy usage is covered by the labor overhead.

8.2 Junction Formation

Junction formation can be divided into six major substeps for the purpose of economic evaluation:

1. Spin-on dopants
2. Diffuse in belt furnace
3. Etch
4. Spray aluminum on back
5. Alloy
6. Post diffusion cleaning

ECONOMIC ANALYSIS OF SURFACE PREPARATION

MATERIALS	
NaOH	0.53¢/wafer
KOH	0.75¢/wafer
Material Total	1.28¢/wafer
EQUIPMENT	
Etch Tanks and Rinsing Stations	0.08¢/wafer
LABOR AND OVERHEAD	
One Operator Required	0.12¢/wafer
Process Total:	1.48¢/wafer

TABLE 8.1.1

The post diffusion cleaning step has been included in this section because its overall cost is minimal in comparison to other processes. The materials, equipment and labor will be identified for each sub-step.

1. Machinery can easily be envisioned which will immerse an entire basket of wafers in dopant solution and spun for a moment to centrifugally remove the excess liquid. In this way a very high volume of wafers can be processed so the equipment cost is neglible. Another major cost savings can be realized by utilizing the Solarex SX-101 dopant costing about 2¢ per wafer. One maintenance operator is also required.

2. Diffusion can be accomplished in a belt furnace with two heat zones. The cells are put individually on the belt and passed through an initial hot zone of 150°C and then through a 950°C zone for six minutes. Based upon the belt furnace at Solarex, which holds 12 wafers in a 48" hot zone at one time, 100 units would be required to be consistent with the required 120 wafers per minute throughput rate. The cost for all of these units would be $660,000, calculated over a five year life time, resulting in a cost of .25¢ per wafer. It is estimated that one operator could supervise the entire diffusion station along with supporting maintenance personnel.

3. Oxides are formed on the wafers during the diffusion process which must be removed in an acid etch. This can be accomplished by immersing wafer filled cassettes in a buffered hydrofluoric acid bath as in surface preparation. Only a five minute resident time is required, however, as compared to a fifteen minute resident time for surface preparation. The hydrofluoric acid costs 80¢ per pound and 0.0022 pounds per wafer are required. This results in a material cost of 0.176¢ per wafer. The equipment cost is estimated at $50,000 for a five year operating life or 0.02¢ per wafer. One person dedicating half of their time to supervising the process would be sufficient.

4. The positive side of the wafers are sprayed with aluminum and a bonding agent in preparation for the back junction alloy. The process consists of passing the wafers under a spray nozzle on a belt transport system. The equipment cost for the whole process can be estimated at $50,000. This implies a cost of 0.02¢ per wafer over a five year lifetime. The materials consist of aluminum powder at approximately 0.2gm/wafer and a bonding agent at approximately 4gm/wafer. Aluminum costs about $17/kg and results in .34¢ per

wafer. A greater proportion of bonding agent is used yet the cost per wafer amounts to only 0.2¢. On a large scale production basis it is estimated that one or two machines could accommodate 120 wafers per minute and would require one operator to monitor the process along with maintenance personnel.

5. The alloying process completes the junction formation step by making an ohmic contact on the back of the cell. As in the diffusion step (#2), a belt furnace with multiple hot zones will be utilized. One hundred furnaces would be required to process 120 wafers per minute at a cost of about $660,000. With a five year lifetime for each machine the cost results in .25¢ per wafer. There are no material requirements for this step and in an automated environment one operator and maintenance support would be sufficient.

6. After completion of junction formation the wafers have residual oxides which must be cleaned for the metallization step.. As in the previous etching baths, a diluted hydrofluoric acid solution is used. Approximately 1cc of fresh solution is required per wafer at a cost of 80¢ per pound. This solution,

along with subsequent rinsing will cost 0.18¢ per wafer. The equipment necessary for wafer transportation between stations and handling equipment at these station will cost about $50,000. Amortized over a five year lifetime this results in 0.02¢ per wafer. One operator supervising the process for only half of the time will be adequate.

Table 8.2.1 summarizes the cost of the junction formation process.

8.3 Metallization

At the onset of this contractual work the cost of metallization had the potential of being prohibitive. Through careful selection of materials and metallization techniques the proposed sequence is well within the budget of 50¢/wafer. Processes such as negative screen printing and solder dipping have been instrumental in maintaining the cost low.

Our proposed metallization technique can be divided into four substeps for the purpose of economic evaluation.

1. Negative Screen Printing
2. Electroless Nickel Plating
3. Edge Removal
4. Wave Soldering

ECONOMIC ANALYSIS OF JUNCTION FORMATION

Substep		
	Materials	
1.	SX-101	2¢/wafer
3	Hydrofluoric Acid	0.176¢/wafer
4	Aluminum Powder	0.34¢/wafer
4	Bonding Agent	0.2¢/wafer
6	Hydrofluoric Acid	0.18¢/wafer
	Materials Total	2.9¢/wafer
	Equipment	
All Wafer Transport		0.03¢/wafer
2	Belt Furnace	0.25¢/wafer
3	Etch Bath	0.02¢/wafer
4	Spray Gun	0.02¢/wafer
5	Belt Furnace	0.25¢/wafer
6	Etch Bath	0.02¢/wafer
	Equipment Total	0.59¢/wafer
	Labor and Overhead	
All Maintenance		0.15¢/wafer
2	Operator	0.12¢/wafer
3	1/2 Operator	0.06¢/wafer
4	Operator	0.12¢/wafer
5	Operator	0.12¢/wafer
6	1/2 Operator	0.06¢/wafer
	Labor and Overhead Total	0.63¢/wafer

Process Total: 4.12¢/wafer

TABLE 8.2.1

This section will summarize the materials, equipment and labor requirements of the metallization process.

1. By applying a negative image of the finger pattern on the wafer great cost savings have been achieved. The resist ink, composed of urethane and titanium dioxide, constitutes the major expense in the process. Four liters of resist can print 1,000 wafers at a cost of about 2¢ per wafer. A stainless steel screen and stencil will cost about $50 each and last for at least 1,000 print cycles yielding a cost of 0.8¢ per wafer. A screen printing machine capable of printing 60 wafers per minute costs about $5,000. Over a three year lifetime the cost of two machines would be $10,000 or 0.01¢ per wafer. One operator would be required at all times to replace screens and to maintain close tolerances in printing.

2. Electroless nickel plating can be carried out in a similar fashion to the etching steps. The nickel plating solution is the principle ingredient and costs about $1.20/liter. One liter will plate 250 4 inch wafers yielding .48¢ per wafer. Once plating is accomplished, the resist ink is removed by immersing the wafer in an organic solvent. One

gallon of resist remover can clean 2,000 wafers which implies a cost of .35¢/wafer. The plating equipment could be a large tank with several hundred slots to accommodate the wafers vertically. This relatively simple mechanism is estimated to cost $50,000 and last over five years. This yields a cost of .02¢ per wafer. The sintering step will assure a good nickel/silicon interface. There are various schemes which could be utilized including heat lamps or small belt ovens. The cost is small in comparison to the other processes. One operator would be required to mix chemicals and monitor the plating tank.

3. The removal of one or two mils of silicon around the circumference of the wafer can be accomplished by mechanical grinding. A silicon or tungsten carbide bit can grind about 2,000 wafers before needing replacement. At $3 per bit the materials amounts to .15¢ per wafer. An automatic grinding machine can be compared in cost to an edge leveling machine used on lenses which typically costs $10,000. Three machines would be required to maintain a 120 wafer per minute rate. This would include cell placement, spinning, and removal along with bit changes and

maintenace. At $30,000 over a three year operating life, the cost of equipment would be .02¢ per wafer. While the machine can step through the grinding operation automatically, an operator would be required to maintain the machine and judge when grinding points need replacement.

4. The use of solder to metallize solar cells, as opposed to precious metals, has allowed the process to remain within the project goals. Yet solder constitutes the largest expense in the metallization process. Solder costs about 10.3¢/cc for 63-37 composition. Each 4 inch solar cell requires 0.48cc to coat both front and back assuming 20% front coverage. Therefore, the materials cost is 4.94¢ per wafer. Wave soldering equipment presently exists that has the capability of coating 120 wafers per minute. This machine is estimated to cost $40,000 and expected to operate over three years. This yields a cost of .03¢ per wafer for wave soldering equipment. One operator would be required to monitor the process.

The costs for the four metallization substeps are summarized in Table 8.3.1.

ECONOMIC ANALYSIS OF METALLIZATION

Substep		
	Materials	
1.	Resist Ink	2¢/wafer
1.	Screen and Stencil	0.8¢/wafer
2.	Plating Solution	0.48¢/wafer
2.	Resist Remover	0.35¢/wafer
3.	Grinding Bit	0.15¢/wafer
4.	Solder	4.94¢/wafer
	Materials Total	8.72¢/wafer
	Equipment	
1.	Silk Screening	0.01¢/wafer
2.	Nickel Plater	0.02¢/wafer
3.	Edge Grinder	0.02¢/wafer
4.	Wave Soldering	0.03¢/wafer
	Equipment Total	0.08¢/wafer
	Labor and Overhead	
1.	Operator	0.12¢/wafer
2.	Operator	0.12¢/wafer
3.	Operator	0.12¢/wafer
4.	Operator	0.12¢/wafer
	Labor and Overhead Total	0.48¢/wafer
	Process Total:	9.28¢/wafer

Table 8.3.1

8.4 Testing

Automatic testing of both mechanical and electrical characteristics can be accomplished by utilizing a minicomputer and other handling equipment. A cell is positioned in a given spot and a series of brushes will test for contact adhesion. The computer then drives a variable power supply to obtain the cell I-V curve.

Microcircuits are contacted through small, closely spaced pads. Precise positioning and delicate application of contacting force is very important. An automatic cell testing machine will cost approximately $100,000. A three year machine life implies a cost of .06¢ per wafer. One operator will be required to monitor the process. Table 8.4.1 presents a summary of testing costs.

8.5 Interconnection and Encapsulation

Panel fabrication has been designed to use readily available and inexpensive materials with a minimum of large equipment. The principle materials include glass, metals and plastics. The selection of glass is a good example of the philosophy with which this project was undertaken. Glass as a superstrate material is one of the most cost effective materials for the production of solar panels. Not only does glass retain high transmission properties for an indefinite amount of time but it serves as a structural support for the entire panel. In the past,

ECONOMIC ANALYSIS OF CELL TESTING

Materials	
0.0	0.0
Equipment	
Cell Tester	0.06¢/wafer
Labor and Overhead	
Operator	0.12¢/wafer
Process Total:	0.18¢/wafer

TABLE 8.4.1

panels have been supplied with frames, then mounted on additional supporting structures. This far exceeds the maximum requirements for safety and support of solar modules. Even more important, the additional cost of providing frames maintains the dollar per watt figure high. Future supporting structures should be designed to meet only those requirements which assure proper stability.

The solar panels will measure 2 feet by 4 feet and contain 55 cells per panel. In order to be consistent with the 120 wafer per minute throughput rate, 2.18 panels per minute must be assembled.

The interconnection and encapsulation technique can be divided into five sub-steps for the purpose of economic analysis. These are as follows:

1. Arc-spray tabs
2. Laminate and outgas
3. Solder tabs on cells
4. Position cells and polyester sheet
5. Reflow

The materials, equipment, and labor will be identified for each sub-step along with their estimated costs.

1. A glass sheet is positioned underneath the arc-spray nozzle and a metal mask is lowered onto the glass. The mask contains 55 slots measuring 1.75" x 0.25" each. Aluminum is sprayed first to form a solid glass/metal interface. Each tab

contains about 4.8×10^{-4} lbs. of aluminum costing $2.40/lb., which amounts to 0.11¢ per Watt. The glass is then passed to the next arc-sprayer which utilizes the same mask and sprays 1.61×10^{-3} lbs. of copper over the aluminum. At $2.88/lb. for copper the cost results in 0.47¢ per wafer. The tabs are then tinned with 8.64×10^{-4} lbs. of solder at $1.00/lb. yielding 0.09¢ per wafer. Each metal can be applied in approximately 20 seconds for the 55 tabs on each panel. Two arc-sprayers will cost approximately $100,000 and will operate 8 hours a day over a three year lifetime which implies a cost of 0.12¢ per wafer. In addition, it is expected that an operator will be required to monitor the continuous flow of glass.

2. The proposed lamination sequence is a three step process consisting of application of two layers of acrylic and an outgassing step. A thin layer of acrylic (5 mils) is sprayed over the face of the cells costing 0.23¢ per wafer. A layer of acrylic resin is then applied measuring 25 mils thick and costing 2.06¢ per wafer. In order to drive all the solvents from the resin the panes of of glass are passed through an oven.

In order to accommodate 2.18 panels per minute the ovens should transport the panels in a vertical direction. In this way 65 panels could be outgassed in each oven at any one time. The cost of two such ovens is estimated at $70,000 amortized over three years results in 0.05¢ per wafer. An operator will also be necessary to oversee this process step.

3. In order to facilitate the interconnection, process tabs are required on the back of each cell. The tabbing process will be accomplished through the use of automated soldering machinery. The only material used is a strip of tinned copper measuring 2 mils x 70 mils x 3 inches and weighing $1. \times 10^{-4}$ lbs. Since the material costs $22.62/lb. the price per wafer is 0.23¢. A fully automated tabbing machine capable of tabbing 120 wafers per minute is estimated to cost $60,000. Calculated over a five year lifetime this amounts to 0.02¢ per wafer. One operator will be necessary to monitor the process.

4. The tabbed cells must now be positioned properly such that the central buss bar of the cells is directly above the arc-sprayed tab on the glass. The tab on the back of the cell must also be positioned so that it contacts the adjacent tab. A polyester sheet

covering the entire panel (8 sq. ft.) is layed over the cells to serve as a backing for the panel. Polyester costs $0.127/sq. ft. which yields a cost of 1.85¢ per wafer. The cost of the equipment required to carry out this process is seen as being negligible as compared to other equipment costs in this process. In addition, it is predicted that no operators will be needed.

5. The combination of glass, acrylic, solar cells, and polyester will be put into a lamination press. This will accomplish two operations simultaneously, 1) interconnect and 2) laminate the entire panel. By applying heat and pressure the solder will reflow thus connecting the buss bar and tab together. Laminating presses are available that can reflow five modules simultaneously at a rate of 20 per hour. Seven machines will be required to accommodate 2.18 panels per minute at a cost of $30,000 each. This yields 0.14¢ per wafer over an expected three year lifetime. One operator will be required to load and unload panels.

A summary of the cost projections for this process is presented in Table 8.5.1. The overall cost of interconnection and encapsulation has been calculated to be 12.69¢ per wafer.

ECONOMIC ANALYSES OF INTERCONNECTION AND ENCAPSULATION

Substep		
	Materials	
1.	Glass	6.84¢/wafer
1.	Spray Al	0.11¢/wafer
1.	Spray Cu	0.47¢/wafer
1.	Solder	0.09¢/wafer
2.	Acrylic Spray	0.23¢/wafer
2.	Acrylic Resin	2.06¢/wafer
3.	Tabbing Material	0.23¢/wafer
4.	Polyester Sheet	1.85¢/wafer
	Materials Total	11.88¢/wafer
	Equipment	
1.	Arc-Sprayer	0.12¢/wafer
2.	Oven	0.05¢/wafer
3.	Tabbing Machine	0.02¢/wafer
5.	Laminating Press	0.14¢/wafer
	Equipment Total	0.33¢/wafer
	Labor and Overhead	
1.	Operator	0.12¢/wafer
2.	Operator	0.12¢/wafer
3.	Operator	0.12¢/wafer
5.	Operator	0.12¢/wafer
	Labor and Overhead Total	0.48¢/wafer

Process Total: 12.69¢/wafer

TABLE 8.5.1

8.6 Summary

A summary of the cost projections for the entire sequence is presented in Table 8.6.1. If the cost for the bulk silicon is assumed to be 22¢ per wafer then the proposed process amounts to 49.75¢ per wafer. Since the power output of these modules was not known at the beginning of the project, one watt per wafer was assumed. It has been determined that cells can already be produced which achieve 794 mW peak power.

This is 82% of the expected power (1 watt), therefore, the cost per watt is presently 62.67¢ per peak watt. Furthermore, we firmly believe that this process has the potential of achieving 12% cells (1 peak watt) with additional optimization and large volume production. At 12% efficiency the overall cost would be approximately 50¢ per peak watt.

SUMMARY OF THE COST ANALYSIS FOR THE ENTIRE PROCESS

Bulk Silicon	22¢/wafer
Surface Preparation	1.48¢/wafer
Junction Formation	4.12¢/wafer
Metallization	9.28¢/wafer
Testing	0.18¢/wafer
Interconnection & Encapsulation	12.69¢/wafer
Overall Total:	49.75¢/wafer
	or
	62.67¢/peak Watt

TABLE 8.6.1

9. Conclusions

This report has described a series of process sequences which we believe have great potential for producing cost effective solar modules, in an automated fashion. Each of the process steps have been designed to readily interface with automated machinery at minimal expense. By following the techniques described herein, we have produced 9.8% efficient solar cells. Furthermore, the cost of automating this process has been estimated at 49.75¢ per wafer.

The successful completion of the last phase of the program, interconnection and encapsulation, clearly demonstrates that our proposed sequence has the potential of meeting the project cost goals. Module fabrication represents the largest expense in the process scheme (12.69¢/wafer), yet it is within the 50¢ per wafer boundary. In addition, this process can be made even less expensive with additional developmental efforts. Continued cooperation between private industry and the government can insure that the LSA goal of 50¢ per peak watt can be realized before 1986. Solarex looks forward to interfacing with JPL in Phase 3 of this contract.

10. Recommendations

There are no specific recommendations at this time.

11. New Technology

There is no new technology to be reported since the third quarter of this contract.